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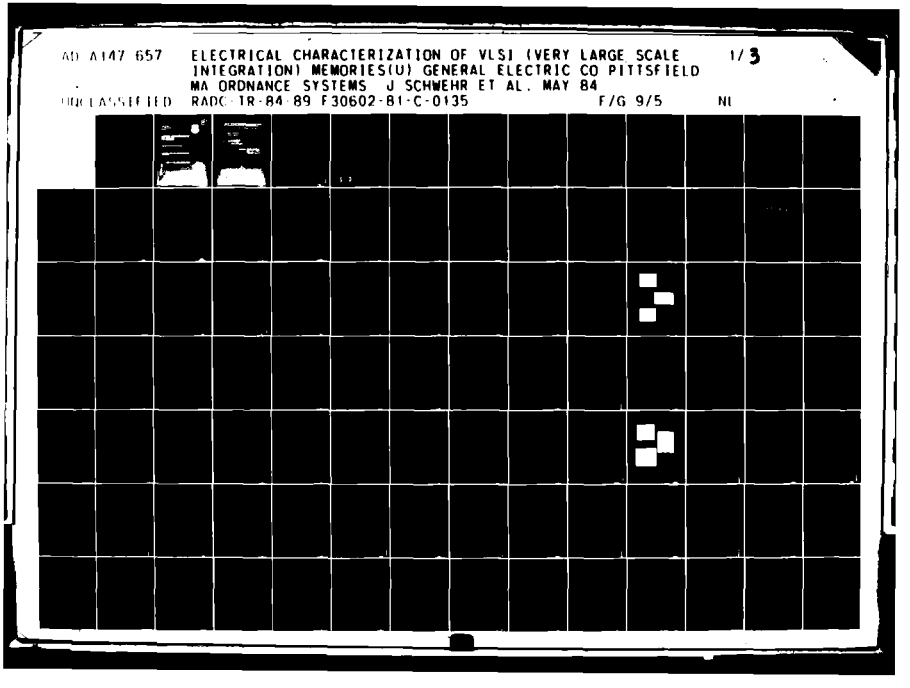

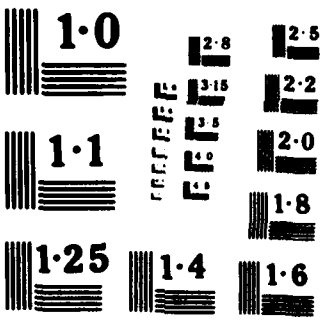
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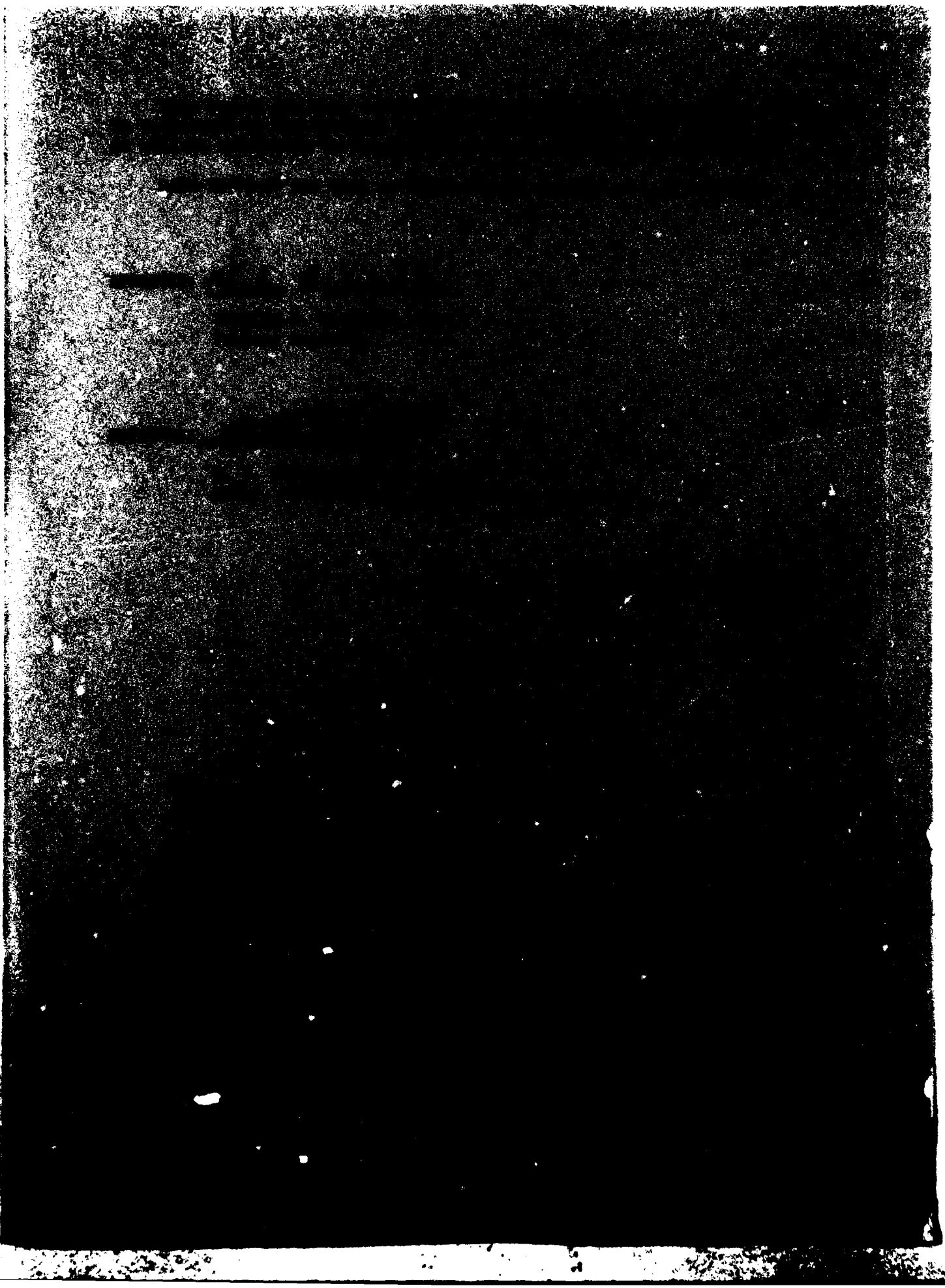

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19 ABSTRACT (Continue on reverse if necessary and identify by block number)

Automatic and bench techniques are used to characterize the performance of several VLSI memory types. The characterization addressed AC, DC, program and erasure parameters over the full military voltage and temperature ranges. Data summaries are presented.

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TERMS AND ABBREVIATIONS

ATE	Automatic Test Equipment
CMOS	Complementary Metal Oxide Semi-Conductor
DIP	Dual In Line Package
DUT	Device Under Test
EEPROM	Electrically Eraseable Read-Only Memory
fmax	Maximum Operating Frequency (PAL16R8)
FPROM	Field Programmable Read-Only Memory
ICC	Supply Current
ICCH	Program Supply Current
IIH	Input Leakage Current Low Level
IIHH	Program Level Input Current
IIL	Input Leakage Current High Level
IOHZ	Output Leakage Current High Level
IOLZ	Output Leakage Current Low Level
IOS	Output Short Circuit Current
IPP	Programming Current
LSI	Large Scale Integration
N-MOS	N-Channel Metal Oxide Semi-Conductor
PAL	Programmable Array Logic
PRAM	Pattern RAM
PROM	Programmable Read-Only Memory
RAM	Random Access Memory
SCA	Socket Card Adapter
SRAM	Static Random Access Memory
TAVCL	Address to Clock Setup Time
TAVEL	Address Setup Time (2K x 8 SRAM)
TAVPH	Address to VPP Setup Time
TAVPL	Address Setup Time (programming)
TAVQV	Address Access Time
TAVWL	Address Setup Time (16K x 1 SRAM)
TAXQX	Address to Invalid Out
TCHAV	Input to Clock Hold Time
TCHAX	Address to Clock Hold Time (16K FPROM)
TCHAX	Input to Clock Hold Time (PAL16R8)
TCHDV	Clock High to Data Valid
TCHEX	Enable to Clock Hold Time
TCHGH	Initialize Recovery Time
TCHQZ	Output Disable Time (16K FPROM)
TCLCH	Clock Pulse Width Low
TCHCL	Clock Pulse Width High
TDVPH	Data to VPP Setup Time
TDVPL	Data Setup Time (programming)
TEHQV	Chip Enable 2 Access Time(32K FPROM)
TELPH	Chip Enable to VPP Setup Time

TELPL	Chip Enable Setup Time (programming)
TELQV	Chip Enable Access Time
TEXCH	Enable to Clock Setup Time
TPHPL	Output Pin Programming Voltage Pulse Width (Vendor E)
TOHQZ	Output Disable Time
TOLQV	Output Enable Access Time
TPHPL	Write Pulse Width
TPLDZ	Data Hold Time (programming)
TPLPH	PGM Pulse Width
TPRC	Programming Voltage RC Time Constant
TELQX	Enable Low to Output Active
TEHQZ	Output Buffer Turn-Off Time
TTL	Transistor-Transistor Logic
TVVPL	VPP Setup Time
UV-EPROM	Ultra Violet - Erasable Read Only Memory
VCC	Supply Voltage
VIC	Input Clamp Diode Voltage
VIH	Input High Voltage
VIHH	Program Level Input Voltage
VIL	Input Low Voltage
VLSI	Very Large Scale Integration
VOH	Output High Voltage
VOL	Output Low Voltage
VOPE	Output Enable Voltage During Programming
VOUT	Programming Voltage on Output Pin
VPH	Voltage to VCC During Programming
VPP	Programming Voltage

EVALUATION

The objective of this effort was to electrically characterize several state-of-the-art semiconductor memories, and using the results then generate draft MIL-M-38510 specifications. The devices selected for this program and their corresponding "slash sheet" numbers are as follows: 16K bit electrically-erasable PROM (EEPROM) organized as 2Kx8, designated /226; enhanced features 16K EEPROM, designated /227; 64K bit ultra-violet erasable PROM (UVEPROM) organized as 8Kx8, designated /223; 32K bit Fusible-Line PROM (FPROM) organized as 4Kx8, designated /211; 16K bit NMOS static RAM (SRAM), organized as either 16Kx1 or 2Kx8, designated /290, and 16K bit CMOS SRAM, organized as 2Kx8, designated /291. Most testing was accomplished using a Tektronix S3270 Automatic Tester; where machine limits were exceeded, bench techniques were employed.

This report contains data summaries and discussions of the characterization results. The specifications which resulted will allow the procurement of reliable military grade products, thereby enhancing the reliability of military systems. The draft specifications themselves are not included in this report; copies can be obtained from the Defense Electronics Supply Center, Dayton OH.

CHARLES H. WINDISCH, JR.
Project Engineer

1. INTRODUCTION

The overall objective of this work was to characterize the following device types and to verify or develop as applicable MIL-M-38510 specifications for these types.

64K UV-EPROM
16K Static RAM
32K FPROM
16 Input programmable array logic (PAL)
16K registered output PROM
16K EEPROM

The characterization task involved the following related efforts:

a. market survey and selection of candidate device types. Device availability and comments that RADC receives from users who have a need for specific militarized components are significant factors in component selection.

b. development of automatic test capability, accumulation and reduction of characterization data.

c. assessment of interchangeability among devices from different vendors.

d. development of preliminary slash sheets based on device analysis and vendor comments.

The development of test procedures includes test pattern sensitivity testing to determine optimum patterns that require short test times but have an effectiveness equal or nearly equal to much longer more exhaustive patterns.

2. TEST CAPABILITY

The development of test capability for each device type was preceded by the generation of a test plan which listed all parameters selected for testing and also listed the temperature, voltage and current conditions. An example of a test plan is contained in APPENDIX A. The test plans not only defined the scope of work to be performed by the test engineers but also served to identify the software and hardware developments that could be applied to more than one device type. The following subsections describe the more significant aspects of the test capability.

2.1 Automatic Test Equipment

Two ATE systems were utilized: the Tektronix S-3270 LSI Test System for the AC and DC parametric testing and the Hewlett Packard(HP)-1000 Data Acquisition System for EEPROM endurance verification. The S-3270 contains an 1804 test table capable of interfacing 64 input and 64 output pins. Capabilities of the GE system that were used on this contract effort include:

a. 14 programmable clock phases (10 drive, 4 compare) with 1ns resolution

b. functional testing at speeds up to 20MHz

c. DC measurements: force V, measure I; force I, measure V

d. device under test (DUT) temperature control from -60° to 160°C

e. data logging and reduction

f. computer graphics display

g. Pattern RAM (PRAM) which can apply predefined test patterns in an algorithmically determined sequence

h. 2942 Programmable Pattern Generator designed to algorithmically generate address and data patterns in sequences especially suited for static and dynamic RAM testing

i. EH1501A pulse generators with delay, width, repetition rate, and rise/fall times programmable via test software

The interface between the DUT and the S-3270 test system was implemented with a socket card adapter (SCA). The SCA mates with the tester and provides a surface area for the DUT socket and for special purpose circuitry to enhance measurement accuracy or provide a unique function required during the test (e.g. a waveshaping circuit for driving the programming pin of an EEPROM).

The HP-1000 Data Acquistion System contains an HP-1000 computer with two hard disk drives. An integral part of the system is an IEEE 488 bus to communicate with compatible equipment such as digital multimeters, signal generators, etc. Also included is a measurement control processor, which with several addressable I/O channels, serves as a general purpose data link to communicate with user designed circuitry.

2.2 Incoming Tests

The incoming tests were designed to identify gross failures of newly received parts. Static RAMs were functionally tested with a data and address pattern that verified cell uniqueness. The 16K EEPROMs and 64K UV-EPROMs were tested after loading with a checkerboard pattern or with the pattern shown in Figure 2.2. The tester's functional comparators were programmed to verify the output logic levels during functional testing. In addition, supply current was measured. Fuselink devices were screened to verify that all fuses were intact. Supply current and the output voltage level resulting from unprogrammed bits were also verified.

2.3 DC Parameters and Conditions

The DC tests for the various device types were selected, as appropriate, from the following list:

input current
output leakage current
input clamp diode voltage
input threshold voltage
output voltage
input/output capacitance

Although listed here as DC parameters, capacitance and thresholds were measured under dynamic conditions. Input/output capacitance was measured while applying an AC signal of 1MHz and 50mVp-p using a Boonton 71A capacitance meter. The remaining DC measurements were done in the classical manner. That is, a specified voltage or current was statically applied and the resulting current or voltage measured. The VCC level was that which provided a worst case measurement.

Input thresholds were measured while applying a dynamic functional pattern, such as marching, to the device. The device cycle times were extended to values that allowed device and system noise transients to settle out before the data from the DUT was checked for accuracy. The pins not currently selected for measurement were given input high (VIH) and input low (VIL) voltage levels of 3.0 and 0.0V respectively. When measuring VIH threshold on a selected pin, VIL was set to 0.0V. Starting with a low and failing value, VIH on the selected pin was incrementally increased at each execution of the dynamic functional pattern until a value was found that allowed the device to pass. That value was designated the VIH threshold.

Similarly when VIL threshold was being determined, VIH was set to 3.0V. Starting with a high and failing value, VIL was incrementally decreased at each execution of the test pattern until the device passed. That value was designated the VIL threshold.

Prior to the DC tests, all programmable parts were programmed with the data patterns developed for AC testing. The data patterns are described in more detail in the section discussing test patterns.

2.4 AC Characterization Techniques

The general philosophy for the development of AC functional characterization capability required that the following be verified or established:

a. output voltage limits under loaded conditions

b. input voltage dynamic operating limits

c. input and output timing limits under dynamic functional conditions

d. functional integrity

e. performance over the -55° to 125°C temperature range and the 4.5 to 5.5V VCC range

During the characterization of a particular timing parameter, all other parameters are set to vendor specified limits or to more optimal values. This criteria insures that as the selected parameter is adjusted toward its operating limit, a failure is due to that parameter. The method used to isolate a parameter limit was the binary search.

2.4.1 Software

2.4.1.1 Binary Search

A classical technique for characterizing an AC parameter involves incrementally adjusting the parameter through a predetermined range and recording a test pattern pass/fail response at each parameter setting. A plot of the responses versus magnitude of the parameter will exhibit the operating limit (pass/fail boundary) but only to the accuracy of the incremental step size. Increased accuracy requires the use of smaller steps, which implies a larger number of test executions. A total of 31 test executions are required if the range is 300ns and the step size is 10ns.

The VLSI memory effort made use of a binary search technique to determine the operating limit of each selected AC parameter. A binary search isolated the parameter pass/fail boundary within a range of values, by repetitively testing the device and eliminating one half of the then current range of values. The half that is eliminated is based on the outcome of the test. The half that is retained encompasses the pass/fail boundary.

The initial range of values for a parameter is made sufficiently wide to guarantee that the operating limit (pass/fail boundary) is enclosed. Therefore the device will fail with the parameter set to one end of the range and is expected to pass with the parameter set at the other end. The value at the "passing" end is equal to the vendor specified limit or to a less stringent value. If a device fails a test at that value, characterization of that parameter is terminated.

When a device passes testing with the parameter set at the passing end of the range, the parameter is set to the middle of the range and tested again. A subsequent pass results in the passing end of the range being pulled in to the parameter value. A failure would cause the "failing" end of the range to be pulled in to the parameter value. This process cuts the range size in half. After readjusting the range, the parameter is again set to the middle of the range before the test pattern is again executed. On each repetition of this process, the range is reduced by one half, but the range continues to enclose the operating limit of the parameter. When the range is 1ns wide, the passing end is the desired worst case operating limit.

The number of steps, n, to reduce a range, r, to x ns can be found through the relationship

$$x(2^{**}n) = r.$$

Therefore,

$$n = (\ln r/x)/(\ln 2).$$

For an r of 300ns and x = 10ns, n would be 4.9. Since n is not an integer, 5 steps would be performed to isolate the value to less than 10ns. This is in sharp contrast to the 31 steps required in the classical approach.

2.4.1.2 Parameter Arrays

In order to standardize S-3270 AC tests which could be used for different memory types, an array driven test was developed. An array containing all necessary timing conditions based on vendor specifications was developed for each device type to be characterized. The test program accesses the appropriate array for the timing information to be applied during the dynamic functional tests. An example of an array is shown in Figure 2.1. Each row in the array contains the timing information and identifies the test routine applied during the characterization of one AC parameter. The first and second columns contain mnemonics and an assigned number that identify the parameter associated with each row. The third column indicates the initial range that the binary search will utilize. The fourth column lists the address test pattern to be applied and the remaining columns indicate the timing conditions of the device inputs and the tester data strobe.

2.4.1.3 Test Patterns

Address Patterns

Several types of address patterns were used for the AC characterization and pattern sensitivity testing. The type of pattern used during a particular measurement depended on the device type, execution time and estimated effectiveness. The patterns selected are identified in the text covering each device type. The following is a list of pattern types used:

March
Address Complement
Row Complement (at each column)
Column Complement (at each row)
Gallop

Appendix C contains a description of the test patterns. Although many RAM and ROM address patterns are the same, the RAM patterns incorporate data patterns for write operations.

Input patterns for the PAL devices do not follow a structured flow as for the ROMs and RAMs. PALs were treated as non-homogenous mixtures of combinational and sequential logic (as they are in application). Thus the input patterns are pseudo random, but exhaustively check all programmed and unprogrammed fuses.

Data Patterns

The data pattern such as that illustrated in Figure 2.2 was applied to each ROM device (except Registered Output PROM). In the figure, Nc represents the maximum column address and Nr the maximum row address. It was ideally suited for the row/column patterns where the column decoder is stable while the row decoder is exercised and vice versa. The pattern is designed such that the 8 bit data word at each column address within a single row is unique. Also, the 8 bit data word at each row address within a single column is unique. Using this data pattern, row/column address patterns such as row and column complement can be used to verify address uniqueness.

For the PAL devices, four separate fuse patterns were developed to collectively verify the ability to program any fuse, verify logic integrity and to verify that fuses left intact are actually conductive. A device can receive only one fuse pattern, but each of the four patterns will be programmed into several devices. These four fuse patterns are displayed in Appendix B.

2.4.2 Hardware

2.4.2.1 Output Loads

Since each vendor guarantees that his device will meet its VOH and VOL specifications, the output loads used during AC testing are designed to provide maximum specified current loading at these voltages. Figure 2.3 illustrates an output load. Resistor RL was selected to provide the maximum load current at the maximum allowed output logic low voltage. RH provides maximum load current at the minimum allowed logic high voltage. The 50pF capacitance includes the parasitic capacitance of the test equipment.

To verify that the outputs reach their specified voltage limits, in an AC environment, the test system detection thresholds were set to those voltage limits during the AC parameters characterization.

```
                MOSTEK DEVICE TEST  4802 8Kx8 ROM        REV.H
COM  VAR  S   :DLT:  PAT :CYC :    UP     :    OE     :    CS     :  DATA  :STR : ADDRESS :
TCA       2   500N   21   600N 160N 250N  0N   550N 150N 435N  0N   550N 510N  0N   550N
TOA       3   500N    2   800N 160N 250N 150N 435N  10N  550N  0N   550N 510N  0N   550N
TWP       6   200N    2   800N 250N 150N  0N   550N  10N  550N  0N   550N 510N  0N   550N
TAS       7   200N   21   800N 150N 250N  0N   850N  50N  750N  0N   850N 750N  0N   850N
TDS       8   600N    2   800N 25N  250N  0N   750N  10N  850N  0N   750N 825N  0N   750N
TAH      10   500N    2   1.0U 500N 250N  0N   975N  30N  850N  0N   975N 450N  0N   525N
TDH      11   500N    2   800N 300N 250N  0N   750N  10N  800N  0N   750N 450N  0N   750N
TCU      16   100N    2   600N 150N 100N  0N   400N  10N  300N 150N  100N 300N  0    150N
TCD      13  -400N    3   1.0U 500N 250N  0N   975N  10N  425N  0N   975N 400N  0N   950N
TWH      17   450N    2   600N 50N  450N  0N   550N 200N  350N  0N   550N 500N  0    550N
TWS      18   250N    2   600N 150N 300N  0N   550N  30N  340N  0N   550N 300N  0N   550N
STOP
```

Figure 2.1 Parameter Array Example

Column Address		0	1	2	3	.	.	Nc
Row Address	0	0	1	2	.	.	.	.
	1	1	2	3	.	.	.	.
	2	2	.					.
	3	.		.				.
	.	.			.			.
	.	.				.		.
	Nr	.	.	.	.	.	.	.

Figure 2.2 ROM Data Pattern

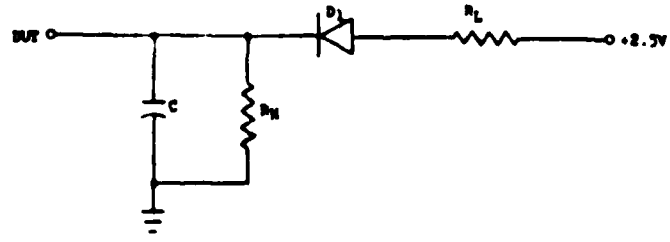


Figure 2.3 Output Load for AC Tests

2.4.2.2 Disable Time Measurement Circuit

Two methods were considered for use in measuring the delay from the output disable (or chip disable) signal to the point at which the DUT output reaches the high impedance state. One method measured the delay from the disable signal to the point at which the output voltage has changed by 0.5V as it transits toward the high impedance voltage from a stable logic output voltage. The high impedance voltage is dictated by the load circuit of Figure 2.3 which was connected to the output when making the measurement. This method of measurement yields values that to a great extent rely on the RC time constant of the output circuit. Once the output does turn off, the voltage on the output is the voltage seen across the load capacitance which discharges through RH or charges through RL and the diode to 2.5V depending on the logic state before cutoff. This method of measurement can be automated and was thus chosen for the MIL-M-38510 draft specifications developed as part of the contract effort. This method does assume an output is disabled (after it has changed by 0.5V) when it may actually still be partially enabled. However, it provides a measurement value that indicates when the output is at a resistive condition that can withstand an externally applied voltage from another device output such as that found on a data bus.

The second method of measurement used the circuit shown in Figure 2.4. This method measures the current flow from the output pin in order to determine the point at which the current falls to zero. During the measurement the DUT output was connected to the load circuit shown in Figure 2.3 via the series resistor RS. The resistor is used to develop a voltage that is proportional to the output current. The resistance was kept relatively small to minimize its effects on the voltage across CL. For most device types RS was 75 ohms when the measurement required the output to transition from a logic zero to a high impedance state and 240 ohms when the measurement required the output to transition from a logic one to the high impedance state.

Figure 2.4 illustrates the scope probe locations for taking the turn off delay measurements. Low capacitance probes were used. Also shown are sketches of the resulting waveforms when both probe signals are superimposed on one another using the identical vertical gain and zero volt reference. Since the difference between probe 1 and probe 2 voltages indicates that output current is flowing, one can determine the point at which the current falls to zero. This is the point at which the output is effectively in the high impedance state.

This method also has an inherent problem. The parasitic capacitance of the device output may continue to discharge long after the output has cutoff. The discharge current through the series resistor is therefore measured as output current by this method. A theoretical analysis has

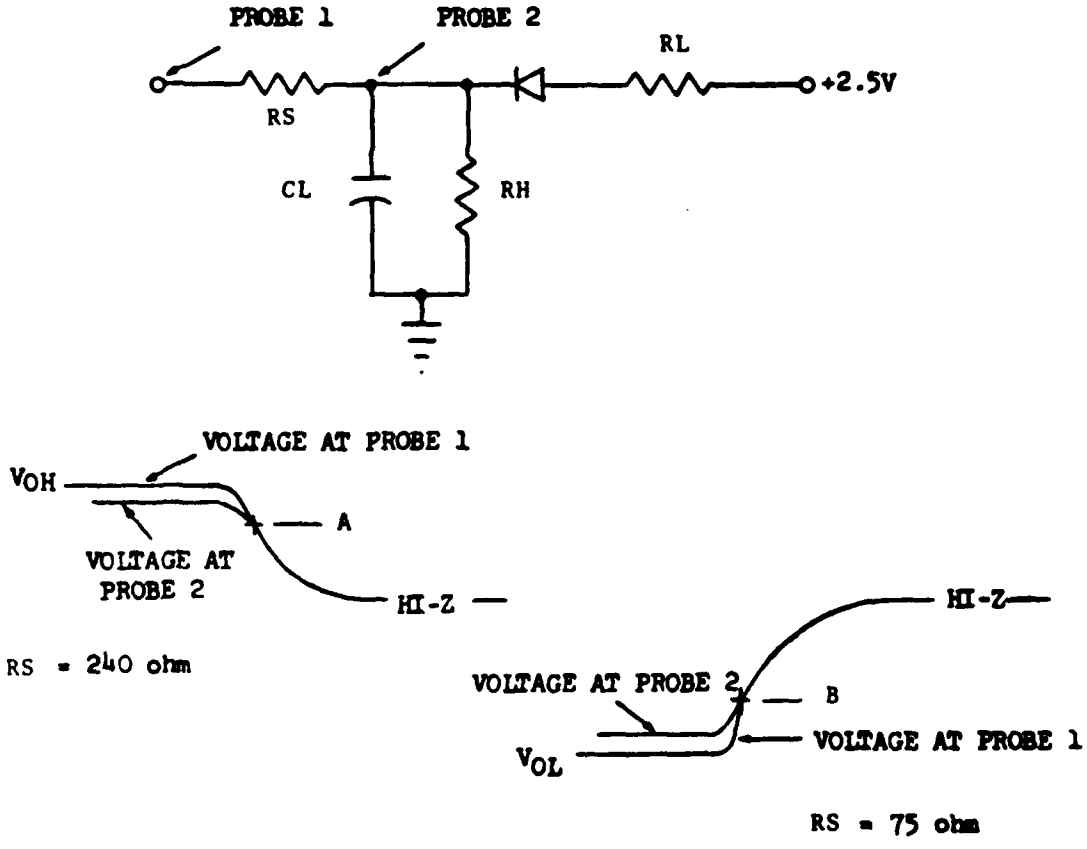


Figure 2.4 Output Load Circuit and Waveforms for Turn-Off Time Measurements

shown that for some various device types and output load conditions, this discharge current can still be flowing after the output voltage has changed by 0.5V, the cutoff reference used by the other measurement method. This current measurement is difficult to automate and experience has shown that some judgement is required in identifying the precise point at which the current stops flowing. In addition great care is required in the calibration of the probes. A small adjustment error results in a significant measurement error. An advantage of this technique is that it yields values indicating when all current flow has stopped, and thus indicates a "worst case" turn off time. The voltage method does not provide a similar worst case number.

Data was taken on all device types using the current measurement technique. For some device types the voltage method was also used. The individual device sections discuss the data.

2.5 Pattern Sensitivity Testing

Several test patterns were utilized to take AC parameter measurements at 25°C in order to identify patterns which result in the greatest access times. The actual patterns used and the results are discussed in the individual device sections. For ROM device types, an underlying objective was to verify that the row/column complement pattern in conjunction with the data pattern like that of Figure 2.2 would be an effective MIL-M-38510 specified pattern for assuring AC and functional performance.

2.6 Programming Characterization Techniques

The objective of the program parameter evaluation was to apply parameter values within and sufficiently beyond the manufacturers' specified limits to verify that the limits are adequate. The verification centered on program pulse width and amplitude. For some devices, time and ease of implementation permitted addressing pulse transition times and associated setup and hold times. The following subsections describe the various hardware techniques that were developed for this phase of the characterization.

2.6.1 EEPROM Programming Circuitry

The programming pulse applied to the VPP pin of the EEPROM requires a leading edge that follows an RC time constant. The circuit in Figure 2.5 was installed on the SCA for the EEPROM in order to apply a selection of rise times to the VPP pulse.

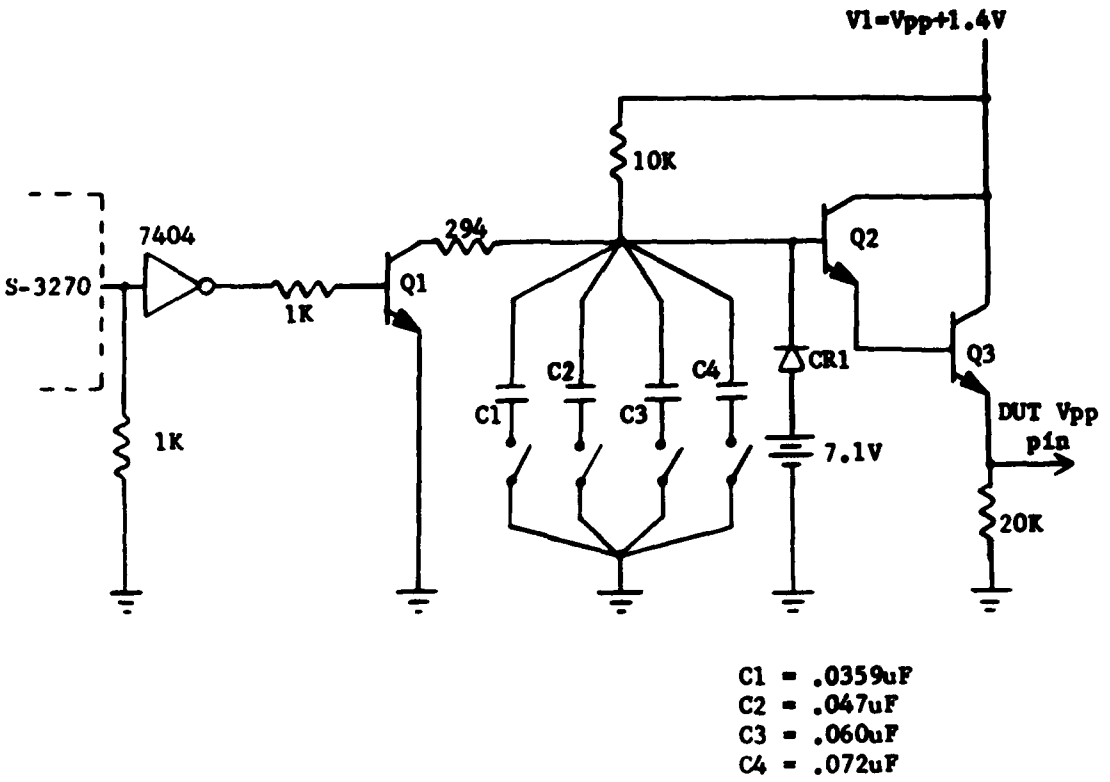


Figure 2.5 EEPROM Programming Circuit

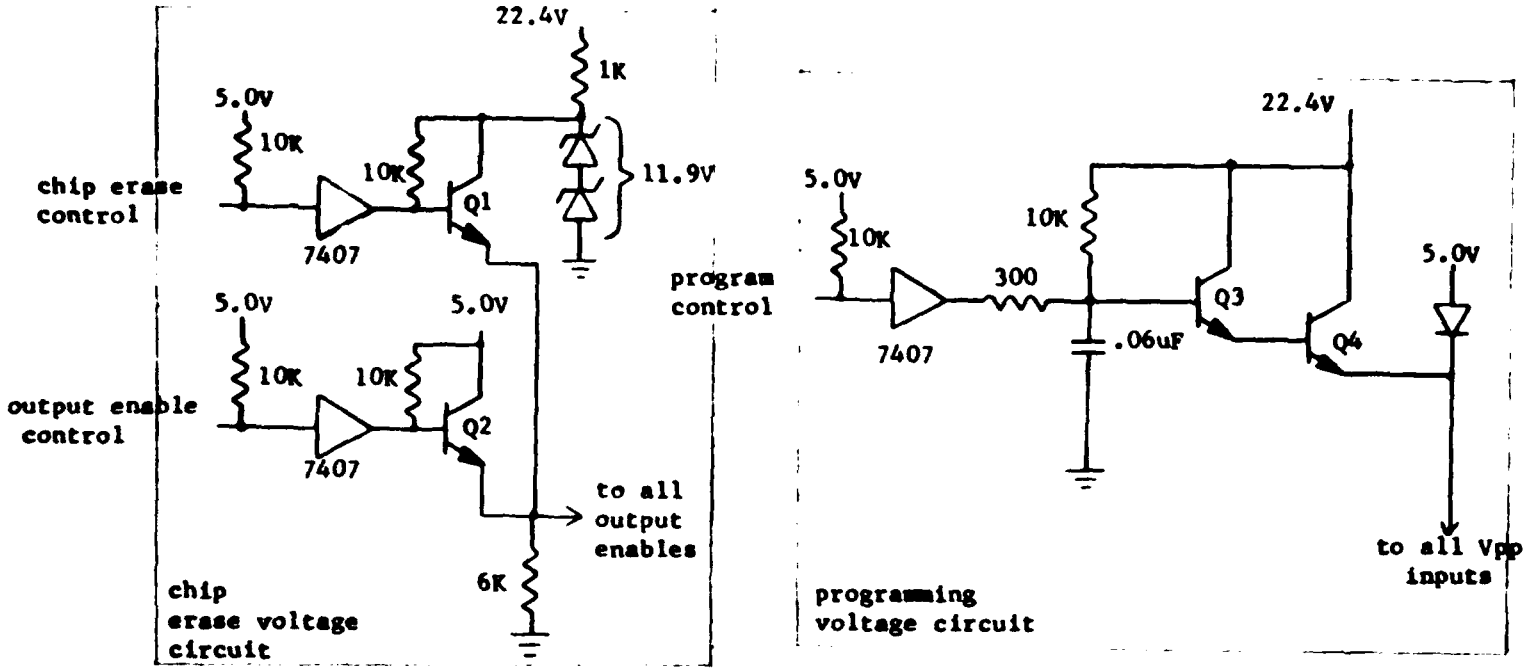
Four capacitor values are independently selected via relays controlled by the S-3270. With Q1 cutoff, the appropriate capacitor charging to V1 through the 10K ohm resistor provides a VPP pulse with the desired rising edge at the emitter of Q3. The width of the VPP pulse is determined by the length of time Q1 is held in the cutoff condition. To terminate the VPP pulse a logic low signal is issued from the S-3270 to the 7404 which in turn, applies a logic high to the Q1 base resistor causing Q1 to conduct. This action quickly discharges the selected capacitor through the 294 ohm resistor. The 294 ohm value was selected to provide a fixed VPP pulse fall time of approximately 10 to 30uS depending on the capacitor selected. The 7.1V supply provides a 5V DC level to the VPP pin in the absence of a programming pulse.

2.6.2 EEPROM Endurance Circuitry

The circuit shown in Figure 2.6 was implemented to interface the HP1000 Data Acquisition System to four EEPROMS during endurance testing. The address, data, VPP and OE pins for each device were all driven from common sources. During a read operation, chip erase, output enable and program control inputs are at logic low values. This cuts off all transistors forcing a logic low at all output enable inputs and a logic high (via the forward biased diode in the programming circuit) at all VPP pins. While enabling a single chip, the address inputs were cycled through all locations and the data outputs were observed for the correct data. Each chip was individually selected and read in this manner.

During a chip erase cycle the output enable control was forced to a logic high value causing Q2 to conduct, placing an approximate 5V level on all output enable pins. All chips were enabled to allow a simultaneous erasure. At the appropriate time in the erase cycle, chip erase control is forced high causing Q1 to conduct, connecting an approximate 11.9V level on the output enable inputs thus initiating an erase of all cells. After the desired length of time, chip erase control is returned to a logic low terminating the erase mode.

To effect a program cycle, a single chip is enabled and the addresses are cycled through all locations. At each address cycle the desired data word is placed on the data I/O bus and the program control input is pulsed high, causing Q3 and Q4 to conduct. The .06uF capacitor charges through the 10K ohm resistor controlling the rise time of the Q3 base voltage and, therefore, that of the VPP pulse. When the program control goes low, the capacitor is quickly discharged through the 300 ohm resistor and the VPP voltage returns to the voltage resulting from the diode clamp. All chips are programmed in sequence.



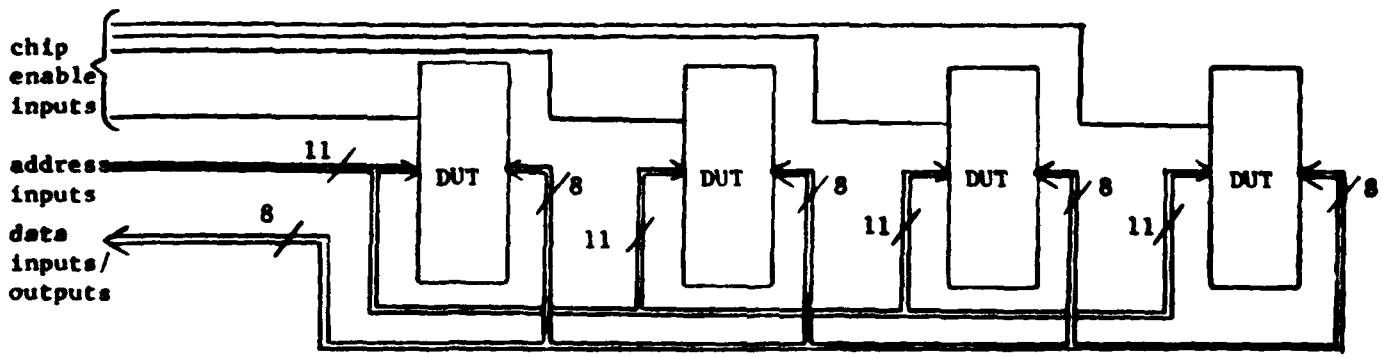


Figure 2.6 EEPROM Endurance Circuit

2.6.3 16K Registered Output PROM Programming Circuitry

The schematic in Figure 2.7 illustrates the circuit used on the SCA to provide the program level voltage pulses to the output pins of the 16K FPROM and the circuit used to supply a bilevel voltage pulse to the VCC pin. A S-3270 driver controlled by the software triggers the EH1501A pulse generator. The generator output pulse, whose parameters are selected by the software, is fed to the non-inverting input of the operational amplifier (op-amp). The op-amp, providing a gain of 2.4 controls the Q1 base voltage and thus controls the voltage applied to the selected output pin via the common bus of the S-3270. The VS7 supply at the collector of Q1 furnishes the bulk of the DUT current.

A second S-3270 driver applies a bilevel voltage to transistor Q2. The VCC pin of the DUT thus sees a bilevel voltage which is normally 5V but quickly pulses to 6V during fuse programming.

2.6.4 PAL Programming Circuitry

The PAL devices required multi-level VCC voltages at approximately 400mA during programming. The circuit in Figure 2.8 was developed to provide the necessary voltage levels and current capability. Four S-3270 drivers were wire OR'd at the base of Q1 as shown. Each driver was programmed to output a pulse of unique level, width and phase. The most positive pulse currently applied sets the voltage seen at the VCC pin. By proper selection of the four pulse parameters, the result at the VCC pin will be similiar to the waveform shown in Figure 2.8.

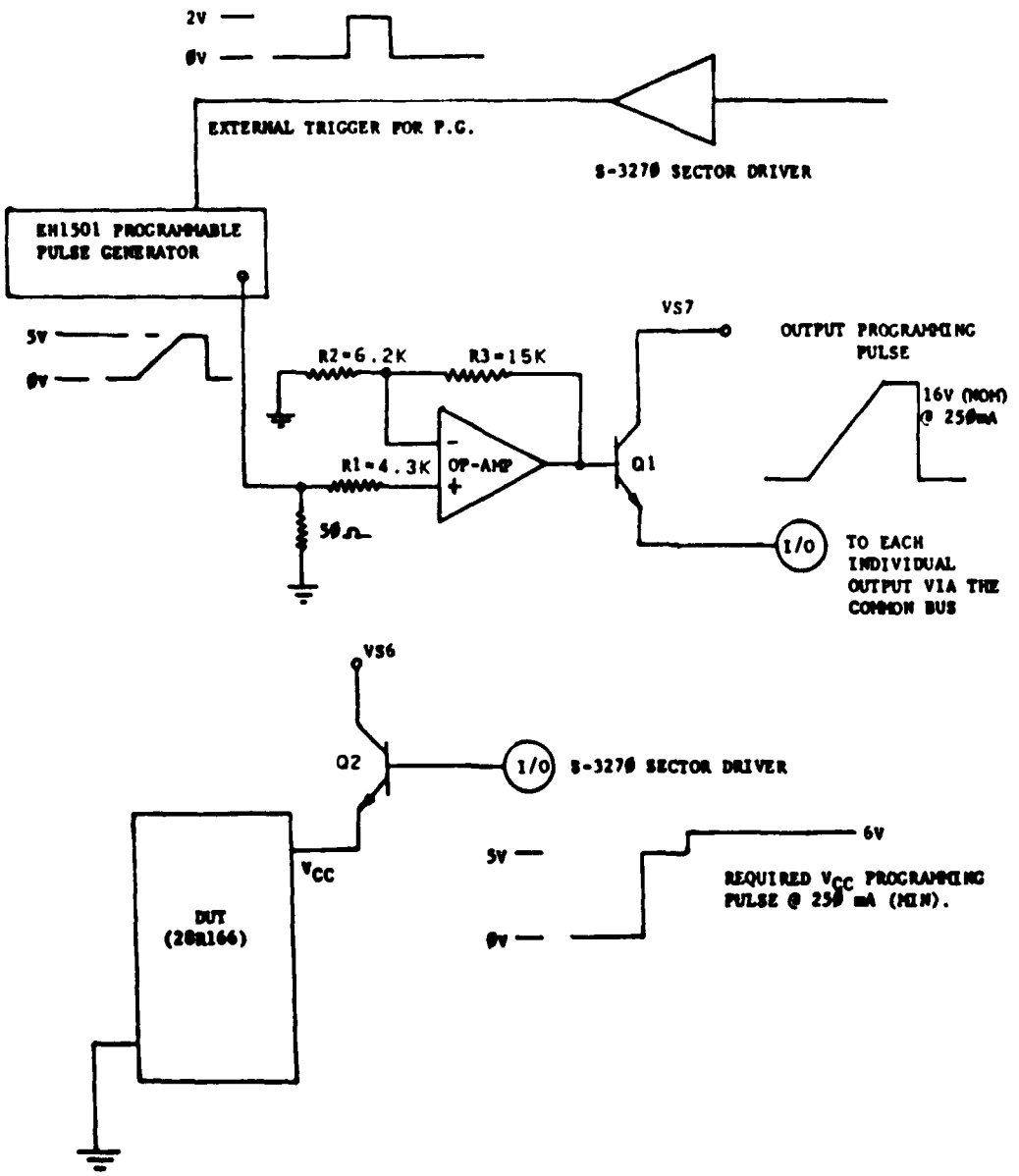


Figure 2.7 16K FPROM Programming Circuit

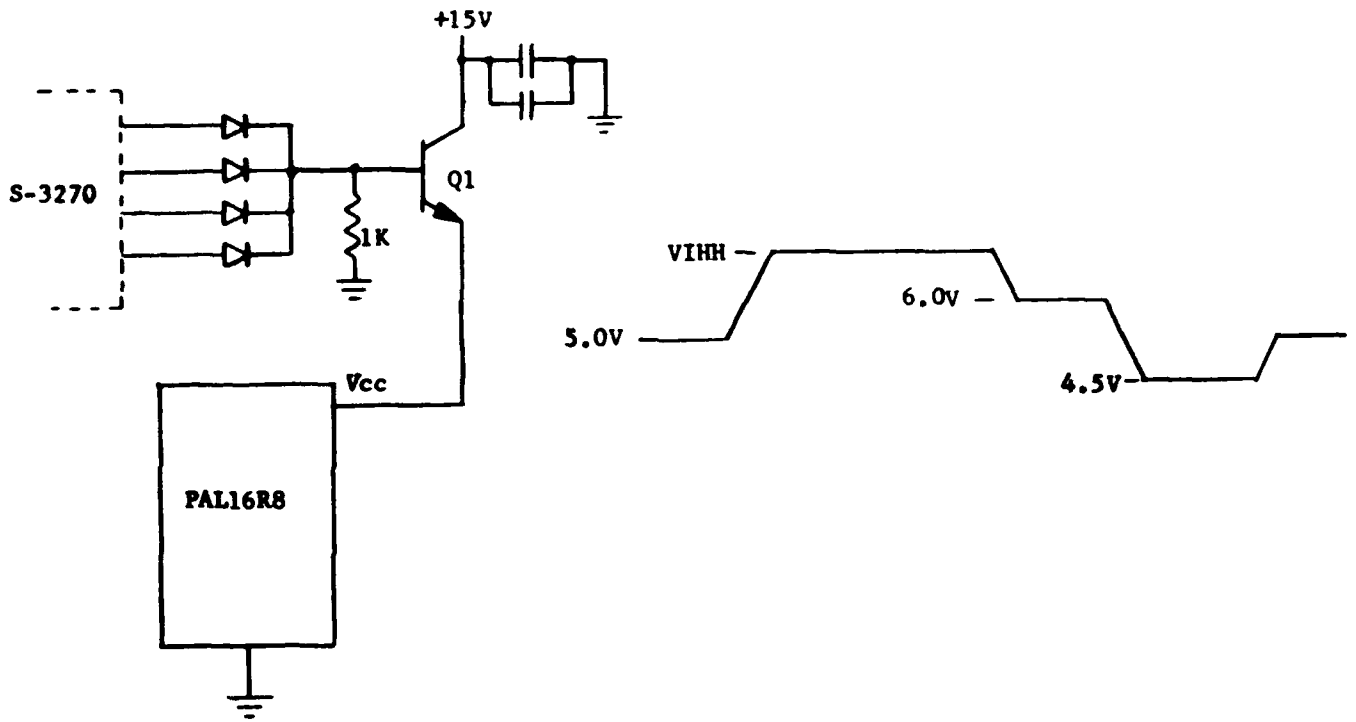


Figure 2.8 VCC Control Circuit for PAL Programming

3. 16K EEPROM

3.1 Introduction

The 2816 EEPROM is a 16,384 bit electrically erasable PROM device ottered by Intel and National. The 2816 has the following special teatures:

1. 10mS bulk or byte erase in PC sockets
2. Programming in PC sockets
   (10mS for byte, 20s for entire chip)
3. Non-volatile storage >10yrs
4. Pin compatible with previous PROMs
5. Moderate access time (250nS)

EEPROM's use a floating-gate tunnel-oxide process. In this process, charge is stored on a polysilicon gate which is surrounded by a silicon dioxide layer. The silicon dioxide layer provides excellent insulation and ensures that charge stored on the gate will remain for long periods ot time(>10yrs). Erasing and writing in the cell is accomplished through a thin oxide layer (200 angstroms thick) using an electron transfer mechanism called Fowler-Nordheim tunneling. This mechanism may be explained as follows: given a sufficient field strength, electrons will jump the forbidden gap and travel from the gate to the substrate. This process is bilateral and therefore can be used to both erase and write into the cell.

From a user point of view, 21 volts must be applied to the device during erasing and writing to provide the necessary field strength. When a low potential is applied across the gate to substrate, the oxide layer acts as a near perfect insulator. Charge stored will remain for greater than 10 years. The device can be read an unlimited number of times without charge degradation. However, the number of erase and write cycles that the device can withstand is not unlimited. After approximately 10,000 cycles, the device's ability to store charge degrades.

The 2816 memory is configured 2K X 8. Information is stored in a 128-row, 128-column matrix. A two line chip-select(CS),output enable(OE) control architecture, similar to the older 2716 UV-EPROM, is used. This type of control architecture allows the device to have a power-down standby mode and the capability to avoid bus contentions.

The 2816 can be bulk erased or byte erased. Both of these operations require a 10mS, 21V programming pulse. The rise time of this pulse must conform to an RC time constant of 600uS (nominal) to prevent damage to the device. Writing and erasing are identical except that during erase, all "1"s are applied to the data lines.

The two vendors characterized were Intel and National. They will henceforth be referred to as Vendor A and Vendor B respectively. Military grade (883B) devices were procured from Vendor A. Vendor B supplied devices tested to the military temperature range (-55° to 125°C). Table 3.1 displays the device quantities received as well as their date codes and access times used in the characterization effort.

Table 3.1 Devices Procured For Characterization

Vendor	Part No.	Access Time	Date Code	Quantity
A	2816	250ns	8210	16
B	2816	250ns	8215	20

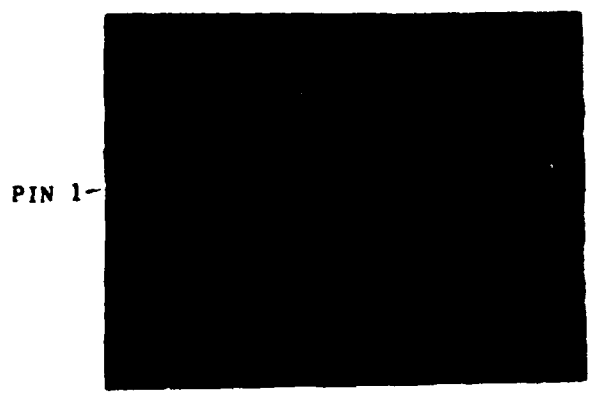
Nine devices were also received from a third vendor. The parts have a specified access time of 350ns. In the read mode the parts function identically to the Vendor A and B parts and can also be programmed in the same manner. The Vendor C parts have an additional feature that allows programming using a logic low level on the VPP pin instead of the 21V pulse required for the Vendor A and B parts.

Upon receipt of the Vendor C devices, all were programmed with the data pattern of Figure 2.2 using the logic low programming voltage on the VPP pin. They were then subjected to the incoming test and passed. Several devices were then programmed using the 21V pulse mode but this resulted in device failure. Subsequent programming using the low voltage mode was unsuccessful. Several of the remaining devices were subjected to an endurance test for 10,000 cycles. Subsequently random bits would change to logic ones several minutes after programming. It was assumed that the failures were due to a loss of the minimum level of charge in the affected cells. This may have been due to cell degradation during endurance testing. Time did not permit fault isolation of either of the two failure modes. Due to the large number of defective devices, further characterization data was not taken.

Photographs of the dies from each vendor are displayed in Figure 3.1. All photographs are to the same scale. Table 3.2 provides a comparison in chip dimensions for the three vendors. The device packages characterized were 24 pin DIPS; the pin configuration is shown in Figure 3.2.

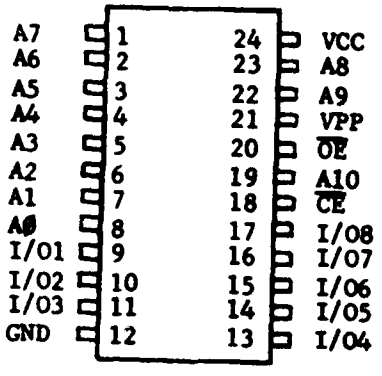
VENDOR A

VENDOR B

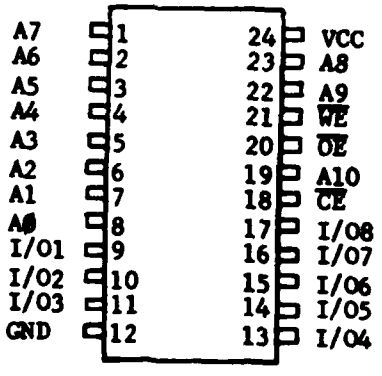


VENDOR C

FIGURE 3.1 DIE PHOTOS - 2K X8 EEPROMs (14.84X)



Vendor A, Vendor B



Vendor C

Figure 3.2 16K EEPROM Pin Configuration

Table 3.2 16K EEPROM Chip Dimensions

Vendor	Length (mm)	Width (mm)	Area (sq. mm)
A	4.95	3.63	17.97
B	5.49	3.20	17.57
C	4.72	3.58	16.92

3.2 Incoming Tests

All Vendor A and Vendor B devices passed the 25°C incoming test described in section 2.2. The data pattern of Figure 2.2 was programmed into each part. The row/column complement patterns were then executed to verify address uniqueness.

3.3 DC Parameters

All DC parameters were measured at seven temperatures: -55, 0, 25, 70, 100, and 125°C. The following parameters were characterized:

1. Supply Current Icc
   standby and active at Vcc=5.5V
2. Input current IIH at VIH = 2.2V
   IIL at VIL = 0.8V
3. Output leakage IOZ at Vin = 0.0V and 5.0V
4. Input/output Capacitance on all pins at 1Mhz
   (25°C only)
5. Input Thresholds VIL and VIH

Table 3.3 lists the DC parameters specified by Vendors A and B.

Table 3.3 Vendor Specified DC Parameters
(Vendors A and B)

PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
VCC	4.5	5.5	V
IIH,IIL		10	uA
IOLZ,IOHZ		10	uA
ICC(ACTIVE)		140	mA
ICC(STANDBY)		60	mA
IPP(READ)		5	mA
VIL	-0.1	0.8	V
VIH	2.2		V
VOL		0.45 IOL=2.1mA	V
VOH	2.4 IOH=-400uA		V

3.3.1 Leakage Current (IOLZ, IOHZ, IIH, IIL)

In general all measurements yielded low currents of 50nA or less and all measurements were well within the manufacturers specifications.

3.3.2 Logic Output Voltage (VOH,VOL)

All devices passed their specified VOH limit at all temperatures including the military extremes. Figure 3.3 summarizes the results for Vendor A and Vendor B. Vendor A's VOH was fairly flat over temperature while Vendor B exhibited a significant increase at -55°C.

All devices also passed their specified VOL limit at all temperatures. Both Vendor A and Vendor B parts displayed a slight linear dependency on temperature. Results are displayed in Figure 3.4.

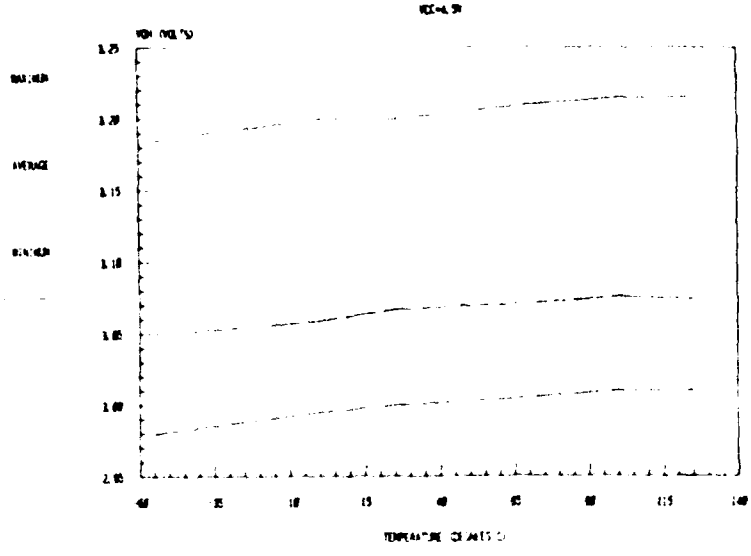


Figure 3.3a Vendor A - Output High Voltage

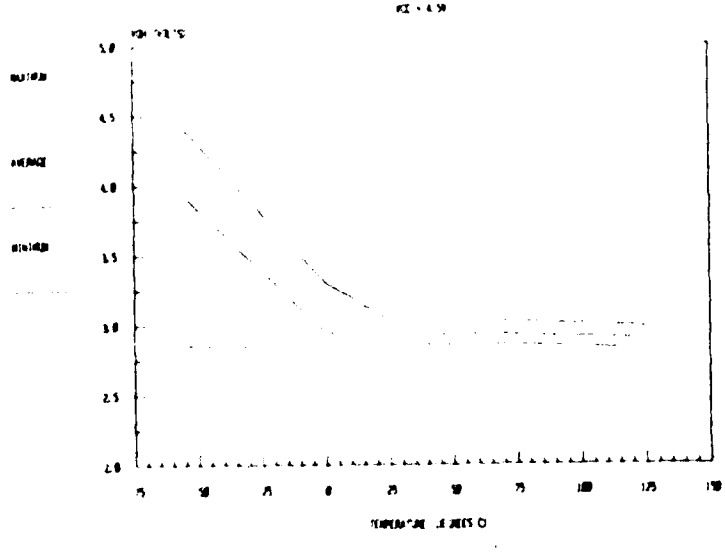


Figure 3.3b Vendor B - Output High Voltage

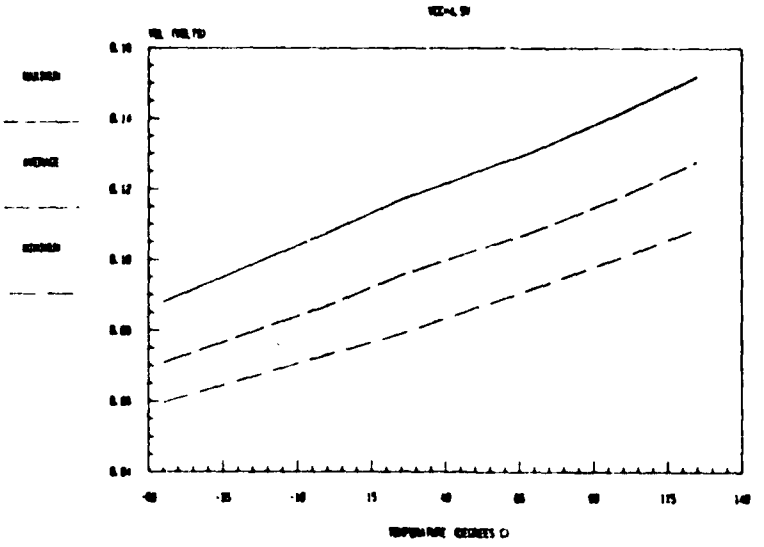


Figure 3.4a Vendor A - Output Low Voltage

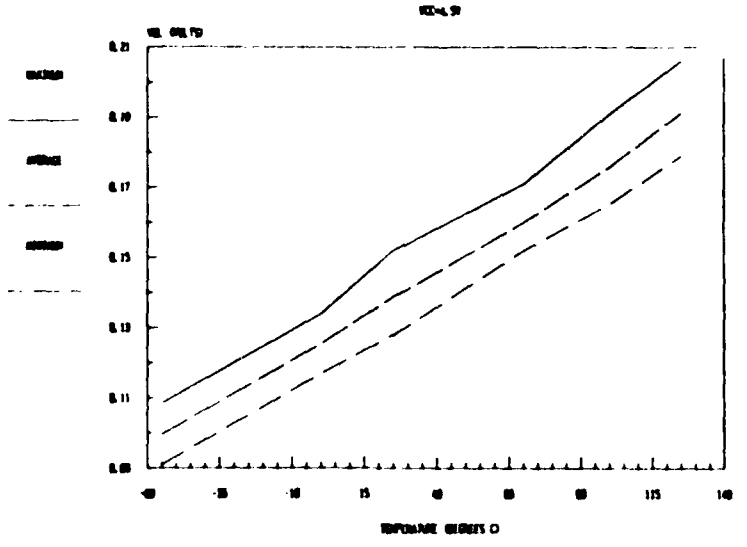


Figure 3.4b Vendor B - Output Low Voltage

3.3.3 Input Threshold Voltage (VIH and VIL)

For the VIL test the input levels were incremented down from 5.0 volts until the threshold was detected. A functional test was run for each increment to determine if the device was functioning properly. Similarly, for the VIH test the input voltage was incremented up from 0V until the threshold was detected. Vendor A and Vendor B's devices passed the test with a worst case VIL of 1.15V.

Both Vendor A and Vendor B devices passed the VIH test. Vendor A's worst case VIH was 1.975V occurring at -55°C. This allows about 0.22V noise margin relative to their 2.2V limit. Vendor B's worst case VIH was 1.85V at -55°C. This resulted in a 0.35V margin from their VIH specified limit of 2.2V. The draft MIL-M-38510 limit was set at 2.0V. As will be described later, the VIH thresholds of the Vendor A devices impacted the AC characterization results. The difference between the worst case VIH and VIL values for both vendors does not indicate hysteresis. The worst case VIH occurred on a different pin than the worst case VIL.

3.3.4 Supply Current(ICC-Active and Standby)

The 2816 EEPROM operates in an active and standby mode. The device is deselected when chip enable(CE) is a logic one. All devices were well below the the spec limit of 60mA for standby current and 140 mA for active current.

Figure 3.5 and 3.6 show min/max/average active and standby current curves for Vendors A and B. Although the active current of the two vendors' devices were similar, Vendor B parts exhibited a standby current much lower than Vendor A. Vendor A's standby current was 22-29mA over the range of temperature, while Vendor B's was below 10mA. Both the active and standby currents exhibit an inverse relationship with temperature as is characteristic of NMOS devices.

3.3.5 VPP Current (IPP-Read)

The programming current IPP was measured with VPP equal to 6 volts, and CE and OE equal to VIH. Both Vendors specify the maximum IPP(read) current as 5mA. All parts passed.

VPP current was also measured with VPP equal to the 22V maximum programming voltage. Figure 3.7 summarizes the results. All parts passed the 15mA limit.

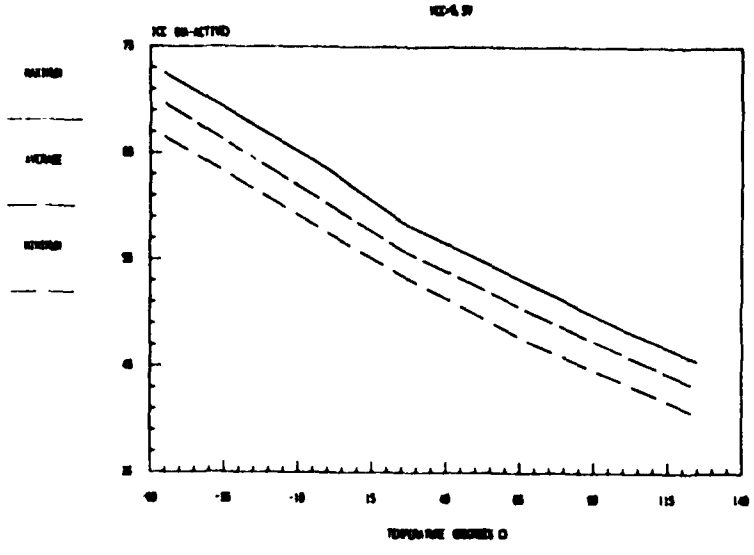


Figure 3.5a Vendor A - Active Supply Current

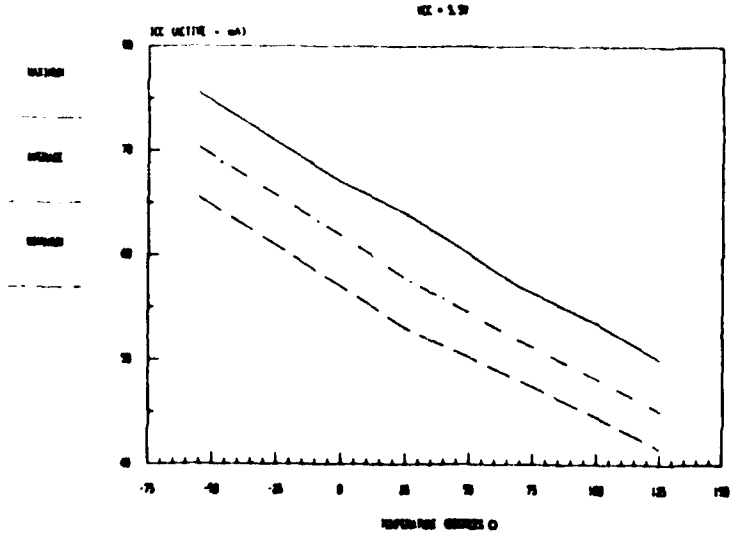


Figure 3.5b Vendor B - Active Supply Current

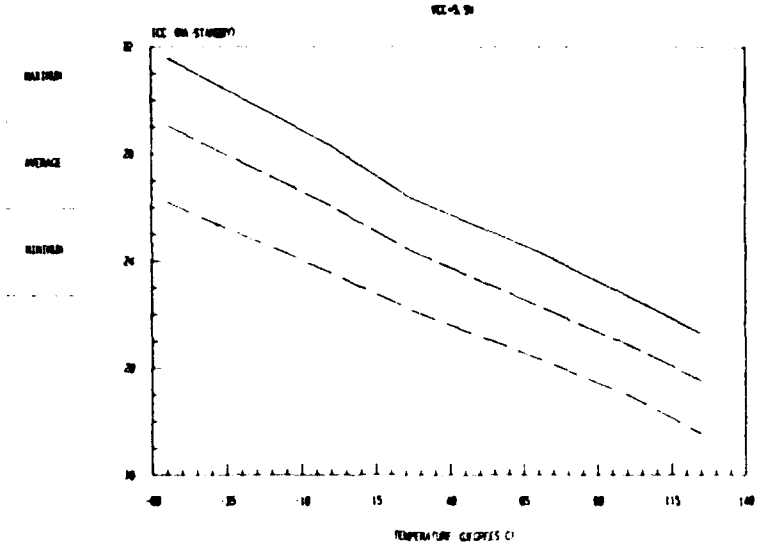


Figure 3.6a Vendor A - Standby Supply Current

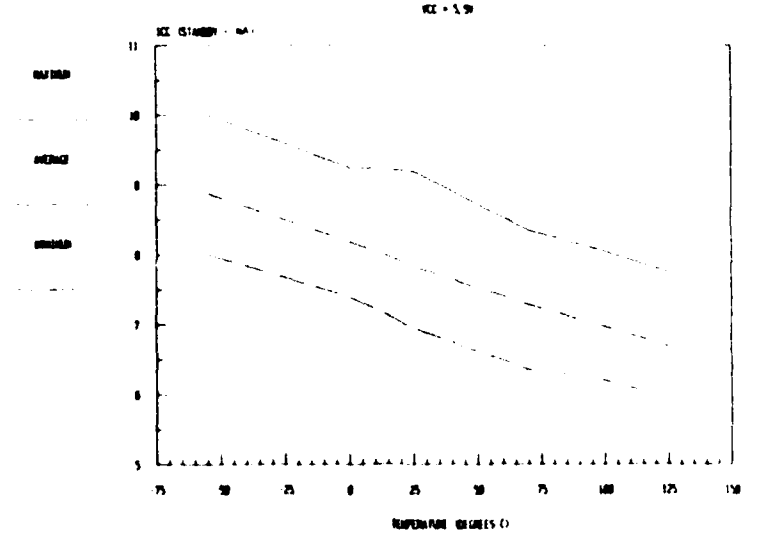


Figure 3.6b Vendor B - Standby Supply Current

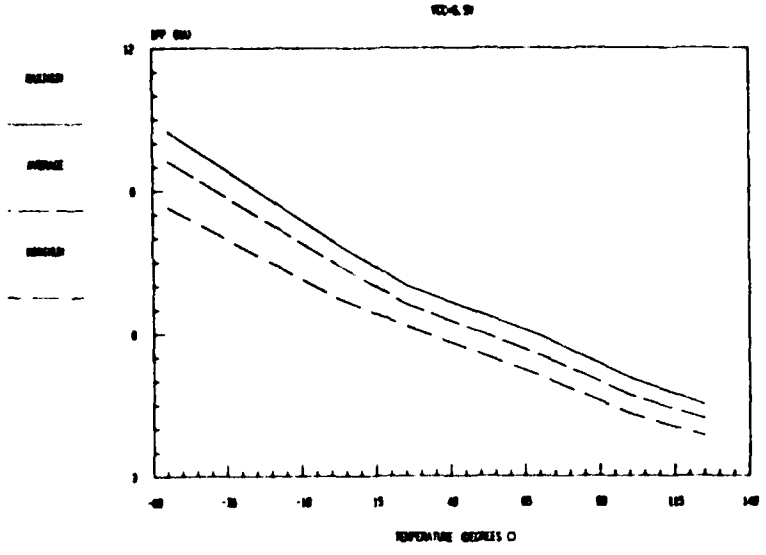


Figure 3.7a Vendor A - VPP Current During Program

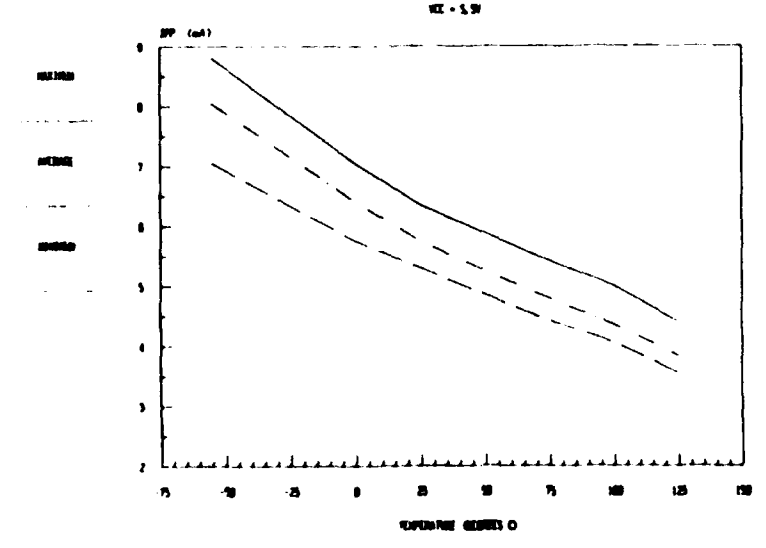


Figure 3.7b Vendor B - VPP Current During Program

3.3.6 Input/Output Pin Capacitance

Capacitance measurements were performed on 5 devices from each of Vendors A and B. Measurements were made from each pin to ground and from each pin to Vcc. Table 3.4 lists the min/max/average measurements for these parts. All measurements were within the manufacturer's limits.

Table 3.4a Vendor A Min,Avg,Max Capacitance

Pin	Pin To Ground			Pin To Vcc			LIMIT
	Min	Avg	Max	Min	Avg	Max	
A0-A10	2.8	3.4	4.8	2.7	3.7	4.8	10pF
I/O1-I/O8	4.6	5.1	6.0	4.5	5.0	5.8	10pF
CE	3.6	3.6	3.6	3.6	3.6	3.6	10pF
OE	4.6	4.6	4.6	4.6	4.6	4.6	10pF

Table 3.4b Vendor B Min,Avg,Max Capacitance

Pin	Pin To Ground			Pin To Vcc			LIMIT
	Min	Avg	Max	Min	Avg	Max	
A0-A10	2.8	3.4	4.8	2.7	3.4	4.8	10pF
I/O1-I/O8	4.6	5.2	5.8	4.6	5.1	5.8	10pF
CE	4.7	4.7	4.7	4.7	4.7	4.7	10pF
OE	3.9	3.9	3.9	3.9	3.9	3.9	10pF

3.4 AC Characterization

All AC parameters except output disable time were tested at seven voltages (4.25, 4.5, 4.75, 5.0, 5.25, 5.5, 5.75) and six temperatures (-55, 0, 25, 70, 100, 125°C). A binary search method was employed to determine the parameter value. The load circuit described in 2.4.2.1 was connected to each output to provide the load during AC testing. Fifteen devices from each of Vendor A and B were characterized. The parameters were tested using an address complement pattern. Pattern sensitivity testing, to be discussed in subsequent text, verified that the address complement pattern was one of several effective patterns for AC characterization. It was selected because its ease of implementation on the S-3270 significantly reduced the characterization time required by multiple test executions. Since address uniqueness had been verified, it was not necessary to use the row/column complement pattern which requires much more S-3270 execution time.

The following parameters were tested:

1. Address Access Time (TAVQV)
2. Chip Enable Access Time (TELQV)
3. Output Enable Access Time (TOLQV)
4. Output Disable Time (TOHQZ)
5. Address To Invalid Out (TAXQX)

Definitions of the AC parameter abbreviations are contained in Appendix B.

Table 3.5 lists the AC parameters characterized along with the manufacturer's specified limits. All AC measurements discussed in this section except TOHQZ were made with output compare levels of 2.4V and 0.4V.

Table 3.5 - AC Characterization Parameters

SYMBOL	PARAMETER	VENDOR A		VENDOR B		
		MIN	MAX	MIN	MAX	
TAVQV	ADDRESS TO OUTPUT DELAY		350		250	nS
TELQV	CHIP ENABLE TO DATA VALID		350		250	nS
TOLQV	OUTPUT ENABLE TO DATA VALID		120		100	nS
TOHQZ	OUTPUT ENABLE TO HIGH IMPEDENCE	0	100	0	80	nS
TAXQX	OUTPUT HOLD FROM ADDRESS	0		0		nS

3.4.1 Vendor A AC Parameters

3.4.1.1 Address Access Time (TAVQV)

The MIL-M-38510 draft specification indicates an address access time of 250ns. Vendor A's own limit is 350ns. The access time summaries of Figure 3.8 indicate that Vendor A devices meet a 250ns limit. The large differentials between each of the minimum, average, and maximum plots illustrates in a general way, a wide variation in device to device performance. Above 0°C the average access time exhibits little sensitivity to VCC.

The Vendor A address access time data (and all Vendor A AC data) was taken at VIH and VIL levels of 2.4 and 0.4V. At 2.0 and 0.8V levels the access time values were inconsistent and excessive. Since their logic high thresholds were very close to the 2.0V logic high level (see 3.3.3), a small amount of tester ground noise caused the logic threshold of the DUT to rise above the 2.0V level being applied. Once this was observed, the logic levels were adjusted to minimize the effect of tester noise.

3.4.1.2 Chip Enable Access Time (TELQV)

Figure 3.9 illustrates the chip enable access time characteristics of Vendor A devices over temperature at VCC=4.5 and 5.5V. As with address access time, the 250ns MIL-M-38510 draft specification limit is met. Here, also, the data illustrates wide variation from device to device. A close comparison between the plots of Figure 3.8 and those of 3.9 indicates that chip enable access time is slightly greater than address access time.

3.4.1.3 Output Enable Access Time (TOLQV)

Figure 3.10 is a summary of the output enable access time data at VCC=4.5V from the Vendor A devices. All parts easily met their 120ns limit. As with other AC parameters, output enable access time increases with temperature which is indicative of increased internal resistances and thus increased time constants. The average data at VCC=5.5V (not displayed) indicates an output enable access times of 5 to 15ns faster than at VCC=4.5 volts.

3.4.1.4 Address To Invalid Out (TAXQX)

This parameter is the delay time from an address change to the point at which the output begins to change (become invalid) from its then current state. The Vendor A specification is 0ns, meaning that in the extreme case the output reaction to an address change is instantaneous.

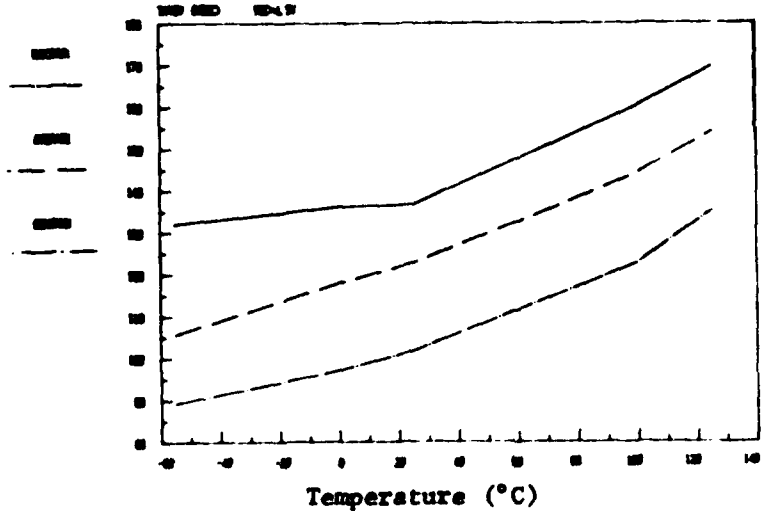


Figure 3.8a - Vendor A Address Access Time (VCC = 4.5V)

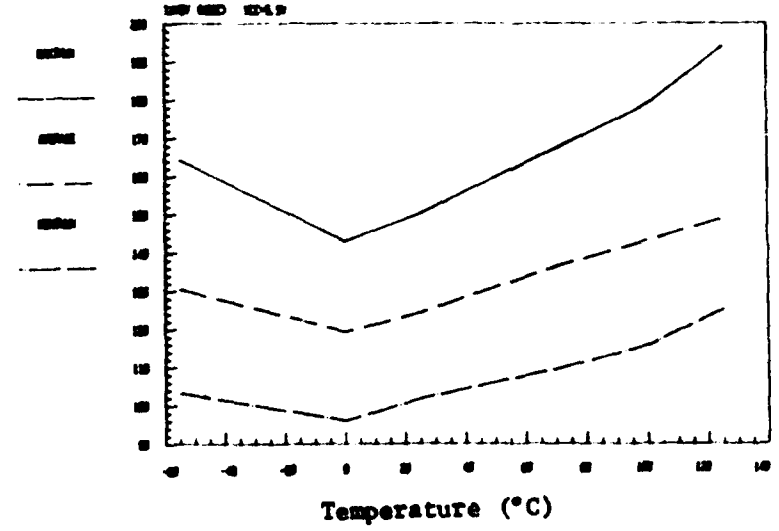


Figure 3.8b - Vendor A Address Access Time (VCC = 5.5V)

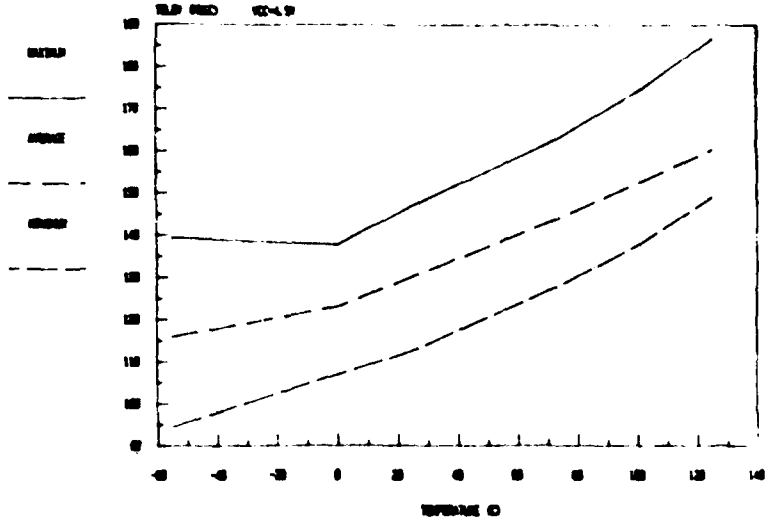


Figure 3.9a - Vendor A Chip Enable Access Time (VCC = 4.5V)

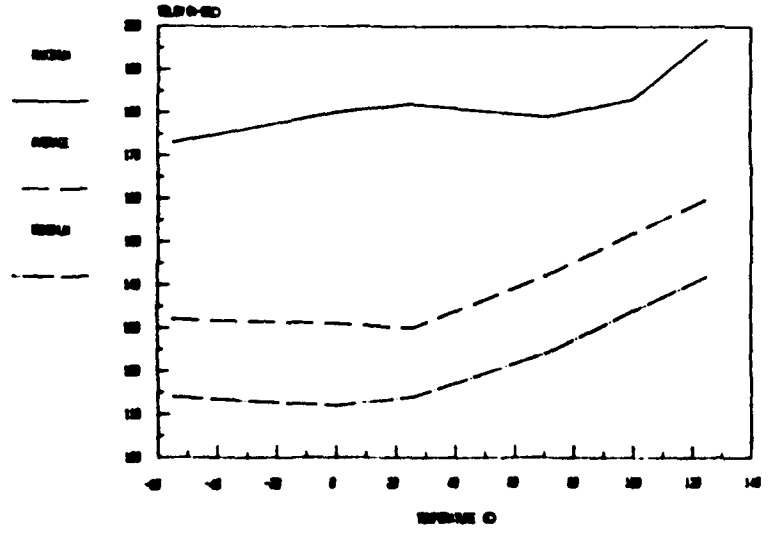


Figure 3.9b - Vendor A Chip Enable Access Time (VCC = 5.5V)

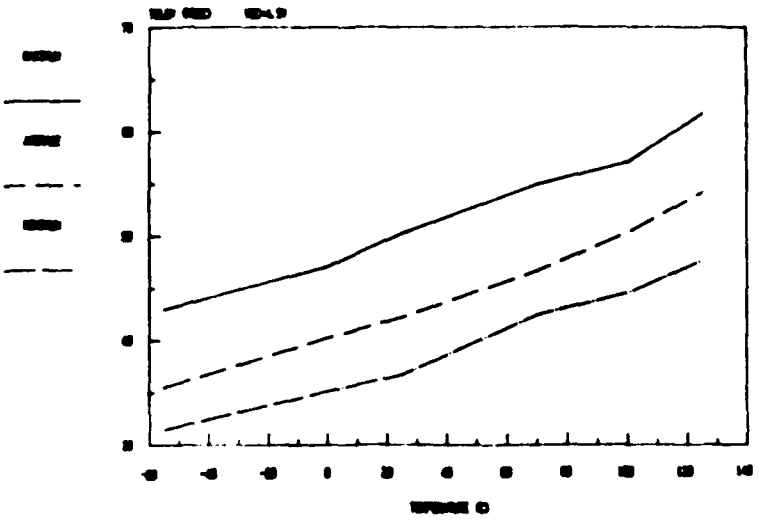


Figure 3.10 - Vendor A Output Enable Access Time (VCC = 4.5V)

During the automatic test, the output was considered invalid when its logic output voltage dropped below 2.4V or rose above 0.4V. At VCC=4.5 and 5.5V the worst case delay was 21ns occurring at -55°C. For both VCCs the average delay was approximately 23ns at -55°C and increased linearly with temperature to an average of 40ns at 125°C.

3.4.1.5 Output Disable Time (TOHQZ)

Data was taken with the bench circuit as described in 2.4.2.2. Both Vendor A and Vendor B specify a turn off delay limit but neither are specific on the criterium for determining when the output is in the high impedance state. The bench data using the current measurement method was taken on ten devices at 25°C. Vendor A devices exhibited delays of 10 to 20ns which are well within the 80ns Vendor and draft MIL-M-38510 specification limit.

The draft MIL-M-38510 specification requires that measurements be taken using the 0.5V output change criterium as described in section 2.4.2.2. This method of measurement will result in values that depend to a great extent on the RC time constant of the load circuit. The worst case time constant occurs when the output is transitioning from a logic high state to the high impedance state. Since the load resistor in this case is 6Kohms and the load capacitance is 50pF, the output will take a minimum of 54ns to transition from 3.0V to 2.5V if the output transistor is cutoff instantly. Any finite turn off delay of the output transistor will increase the transition time. The 3.0V value is the approximate average value across the entire temperature range for Vendor A devices. Even though the actual turn off time is less than or equal to the 10 to 20ns measured on the bench, the measurement criterium in the MIL-M-38510 document requires a limit at least greater than 54ns (greater if the actual VOH level is lower than 3.0V).

3.4.2 Vendor B AC Parameters

3.4.2.1 Address Access Time (TAVQV)

Figure 3.11 summarizes the address access time data for the Vendor B devices at VCC=4.5 and 5.5V. Except for the unusual behavior of one device the data indicates a much smaller variation from device to device than shown by Vendor A data. This data and all AC data for Vendor B was taken while applying logic levels of 2.0 and 0.8V for VIH and VIL respectively. Sample data taken at other logic levels did not differ significantly from the corresponding data at 2.0 and 0.8V. It was concluded, therefore, that Vendor B parts were not as susceptible to tester noise as were Vendor A parts. As described in section 3.3.3, the Vendor B devices have a logic high noise margin that is slightly better than Vendor A devices.

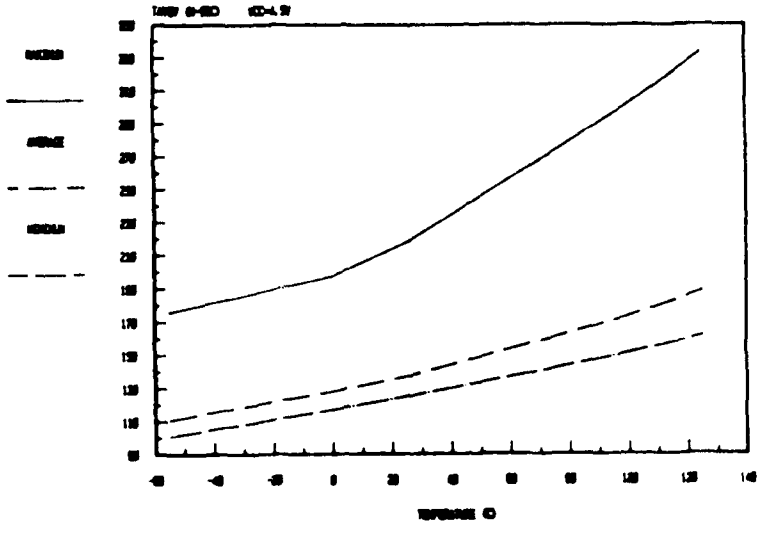


Figure 3.11a - Vendor B Address Access Time (VCC = 4.5V)

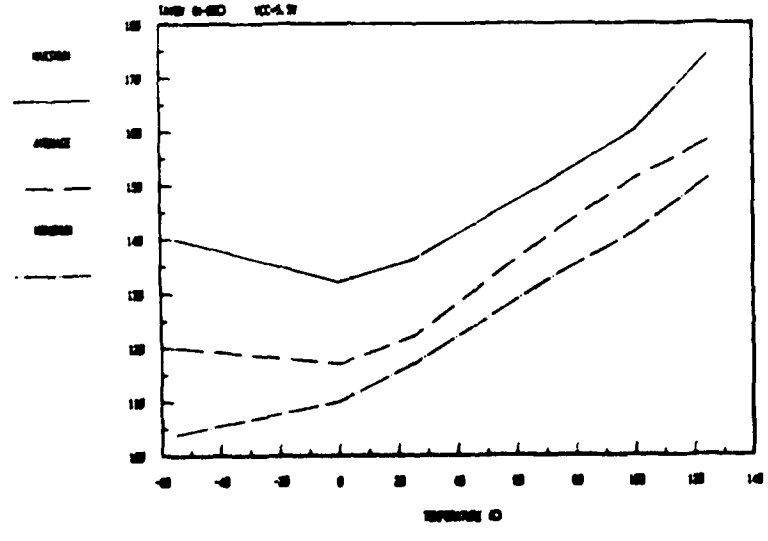


Figure 3.11b - Vendor B Address Access Time (VCC = 5.5V)

3.4.2.2 Chip Enable Access Time (TELQV)

The chip enable access time data from the 15 Vendor B devices at VCC=4.5 and 5.5V is summarized in Figure 3.12. As with address access time, Vendor B parts show less device to device variation than Vendor A parts. Chip enable access times are also somewhat greater than address access time, as they were for Vendor A.

3.4.2.3 Output Enable Access Time (TOLQV)

The summaries of data taken at VCC=4.5 and 5.5V in Figure 3.13 indicate that Vendor B output enable access time is significantly influenced by VCC. Except for one device, the parts do meet the 120ns limit.

3.4.2.4 Address To Invalid Output (TAXQX)

Figure 3.14 illustrates performance of the address to invalid out delay at VCC=4.5 and 5.5V over temperature. The influence of temperature was much more significant for Vendor B parts than for Vendor A parts. For VCC=5.5V, the average value at 125°C, 61ns, is nearly 30ns greater than at -55°C. The Vendor A change between temperature extremes was only 17ns.

3.4.2.5 Output Disable Time (TOHQZ)

Data taken on 10 Vendor B devices at 25°C with the bench circuit described in 2.4.2.2 yielded measurements of 10 to 20ns. As discussed in 3.4.1.5, the method defined in the MIL-M-38510 utilizes a 0.5V output voltage change criterium described in 2.4.2.2.

3.5 Pattern Sensitivity Testing

Table 3.6 summarizes the address and chip enable access time data taken with three different address patterns at 25°C from six devices of each Vendor. Vendor A logic input levels were set to 2.4 and 0.4V for VIH and VIL respectively. Vendor B input levels were 2.0 and 0.8V.

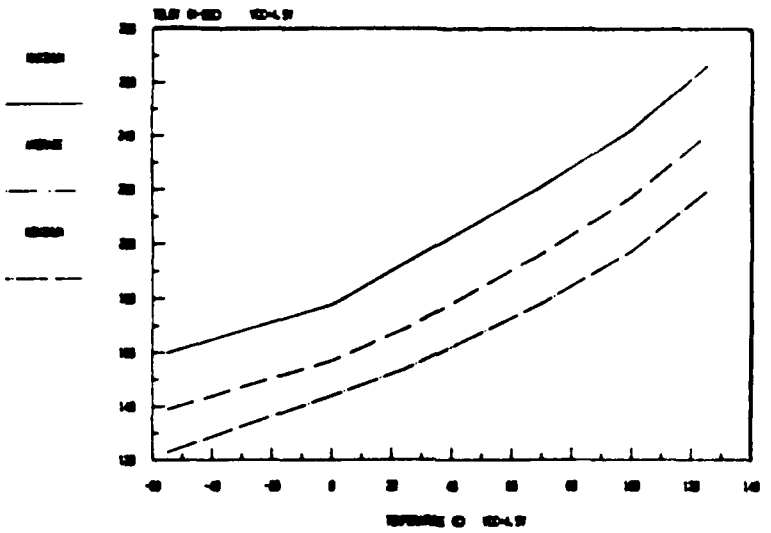


Figure 3.12a - Vendor B Chip Enable Access Time (VCC = 4.5V)

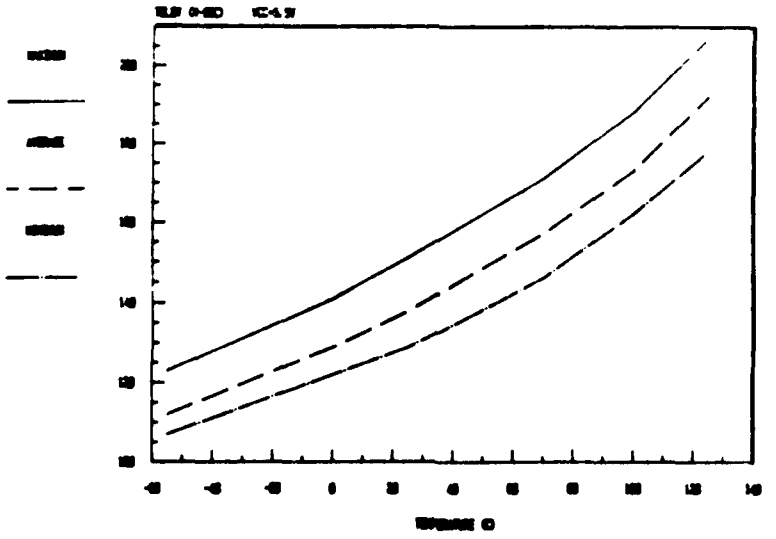


Figure 3.12b - Vendor B Chip Enable Access Time (VCC = 5.5V)

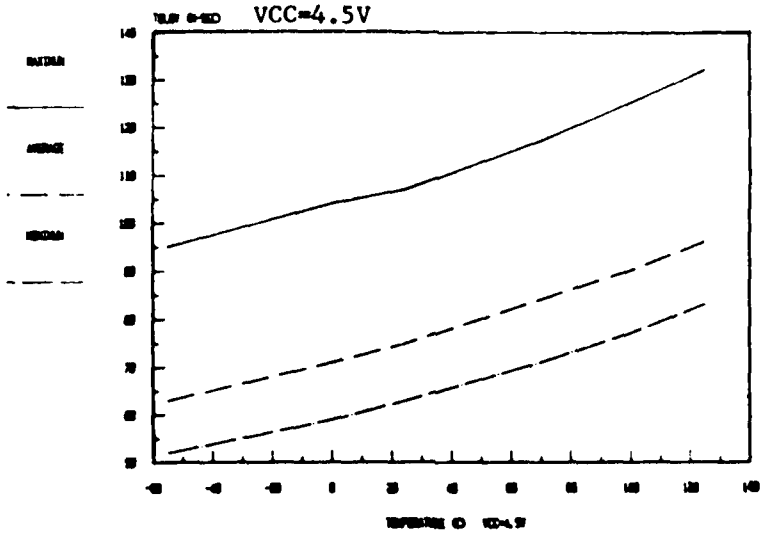


Figure 3.13a - Vendor B Output Enable Access Time (VCC = 4.5V)

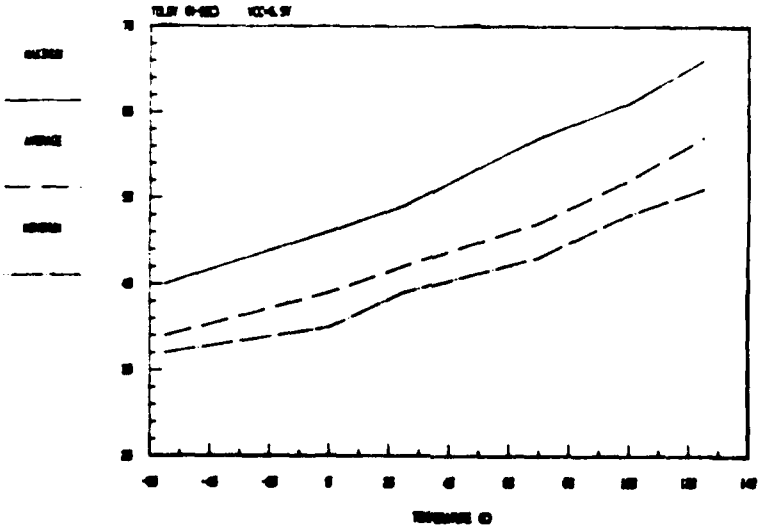


Figure 3.13b - Vendor B Output Enable Access Time (VCC = 5.5V)

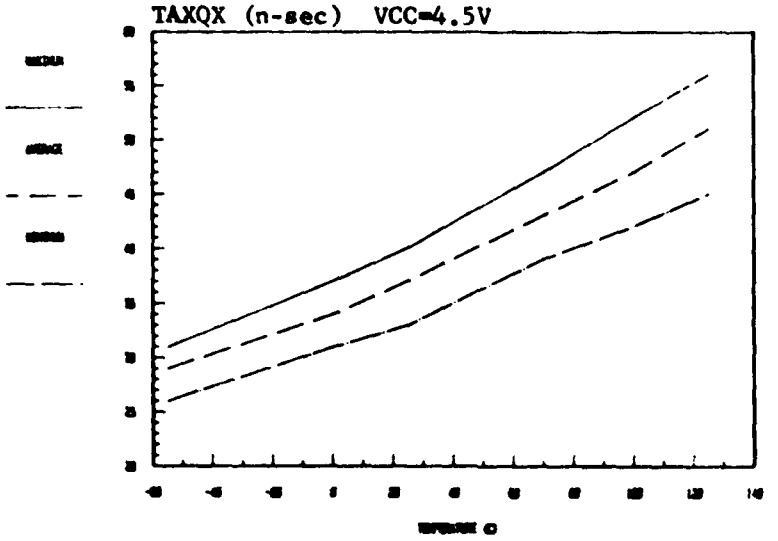


Figure 3.14a - Vendor B Address to Invalid Out (VCC = 4.5V)

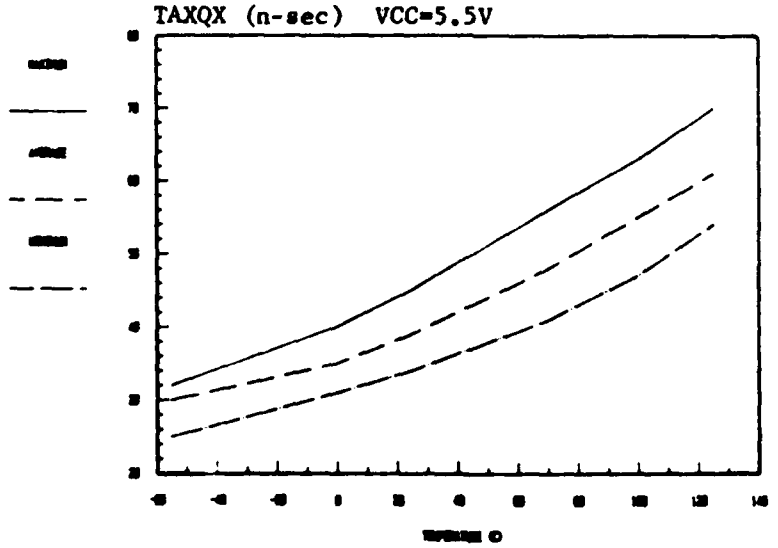


Figure 3.14b - Vendor B Address to Invalid Out (VCC = 5.5V)

Table 3.6 Pattern Sensitivity Result Summary (average of six devices)

	Gallop		Address Complement		Row/Column Complement	
VCC	4.5	5.5	4.5	5.5	4.5	5.5
Vendor A						
TAVQV	126ns	125ns	126ns	121ns	127ns	119ns
TELQV	135	130	130	125	128	124
Vendor B						
TAVQV	137	125	133	122	134	124
TELQV	172	140	170	138	170	138

Although row complement and column complement are two distinct patterns, they were always treated as a single pattern set and run concatenated. The access time values given in Table 3.5 are the worst case values that allow both row and complement patterns to pass.

Vendor A devices show slightly more sensitivity to Gallop than to the other two patterns. The sensitivity was not considered significant enough to warrant inclusion of the pattern in the MIL-M-38510 draft specification. Vendor B devices show almost negligible differences in data taken with the three patterns.

The row/column complement patterns were specified in the draft specification because a single execution of both is fast (equal to 8192 x cycle time) and will verify address uniqueness when used with the data pattern described in 2.4.1.3.

3.6 Programming Parameters

The objective of the programming parameter evaluation was to verify adequacy of the manufacturers' limits. These are listed in Table 3.7. Various programming parameter conditions were applied to each of five devices from both vendors. The values selected for each parameter are as follows:

1. Programming Voltage RC Time Constant (TPRC)
   359uS,470uS,600uS,720uS
2. Programming Voltage (VPP)
   18V,20V,21V,22V
3. Write Pulse Width (TPHPL)
   5mS,9mS,10mS,11mS
4. Address to VPP Setup Time (TAVPH)
   75nS,100nS,125nS,150nS
5. Chip Enable to VPP Setup Time (TELPH)
   75nS,100nS,125nS,150nS
6. Data to VPP Setup Time (TDVPH)
   -25nS,0nS,25nS,50nS

Table 3.7 Vendor Specified Limits for Programming Parameters

PARAMETER	VENDOR A		VENDOR B		UNITS
	MIN	MAX	MIN	MAX	
TPRC	450	600	450	600	nS
VPP	21	22	21	22	V
TPHPL	9	15	9	15	mS
TAVPH	150		150		nS
TELPH	150		150		nS
TDVPH	0		0		nS

While the selected values for one parameter were applied, all other parameters were held at their respective nominal values. The conditions listed above were applied at VCCs of 4.5, 5.0, and 5.5V at temperatures of 25, -55, and 125°C. Table 3.8, which summarizes the results, indicates that the vendor programming limits are more than adequate.

Table 3.8 Vendor A, Vendor B - Number of Passing Devices for Various Programming Conditions at VCC = 5V.

Parameter (at fixed value)	Vendor A # of passing devices			Vendor B # of passing devices		
	-55°C	25°C	125°C	-55°C	25°C	125°C
TPRC (359us)	5	5	5	5	5	5
TPRC (470us)	5	5	5	5	5	5
TPRC (600us)	5	5	5	5	5	5
TPRC (720us)	5	5	5	5	5	5
VPP (18V)	4	3	5	4	4	5
VPP (20V)	5	5	5	5	5	5
VPP (21V)	5	5	5	5	5	5
VPP (22V)	5	5	5	5	5	5
TPHPL (5ms)	4	4	5	4	4	4
TPHPL (9ms)	5	5	5	5	5	5
TPHPL (10ms)	5	5	5	5	5	5
TPHPL (11ms)	5	5	5	5	5	5
TAVPH (75ns)	3	5	5	5	5	5
TAVPH (100ns)	5	5	5	5	5	5
TAVPH (125ns)	5	5	5	5	5	5
TAVPH (150ns)	5	5	5	5	5	5
TELPH (75ns)	5	5	5	5	5	5
TELPH (110ns)	5	5	5	5	5	5
TELPH (125ns)	5	5	5	5	5	5
TELPH (150ns)	5	5	5	5	5	5
TDVPH (-25ns)	5	5	5	5	5	5
TDVPH (0ns)	5	5	5	5	5	5
TDVPH (25ns)	5	5	5	5	5	5
TDVPH (50ns)	5	5	5	5	5	5

3.7 Chip Erase

Chip erase is achieved by raising the output enable to 9V, enabling the device and applying VPP for a specified duration while the data inputs are held at logic '1'. Since chip erasure depends basically on the duration of the write pulse width (TPHPL), the following test sequence was applied:

1. Program device at 9ms VPP pulse width.
2. Erase device at 9ms VPP pulse width.
3. Program device at 70ms VPP pulse width.
4. Erase device at 9ms VPP pulse width.

Two conditions (vendor minimum and maximum limits) of VPP were applied while programming to obtain the best and worst case amount of charge in the programmed cells. The minimum limit of VPP during erasure proved to be adequate to completely erase all cells.

3.8 Endurance

Four devices from each vendor were tested for endurance. This test consisted of cycling the devices 10,000 times. Each cycle was comprised of the following sequence:

1) Erase (all cells in '1' state)
2) Verify erasure (every 250th erasure cycle)
3) Program (all cells in '0' state)
4) Verify program (every 250th program cycle)

It was surmised that if a true endurance failure occurred it would be due to a 'stuck at' condition in one or more cells. For this reason and because of data recording limitations, the programming and erasure verification was performed every 250th cycle. In this way the 'hard' failures that occurred in previous cycles would still be present when verification was performed.

Vendor A and Vendor C devices were subjected to the endurance test and displayed no cell failures over the 10,000 cycles. At the first program verification (after 250 cycles), numerous failures were detected in Vendor B devices. The failures were not repeatable at each consecutive 250th cycle verification and the failures that were detected were not necessarily the same as detected in previous verifications. Since the failures were inconsistent, it is assumed that they were not related to cell endurance. It is suspected that the failures were due to a defect in the internal programming circuitry.

3.9 Bake

A 150°C bake cycle was applied to six devices from each of Vendors A and B. The total time at 150°C was 96 hours. The data pattern in Figure 2.2 was programmed into each device prior to the bake. Subsequent functional testing at 25°C verified that all devices continued to retain the correct data pattern.

4. 32K FPROM

4.1 Introduction

The 32K FPROM is a 32,768 bit schottky, bipolar, field programmable read-only memory configured 4K X 8. Features include dual chip enable controls, tri-state outputs, and single +5V operation in the read mode. The tri-state data outputs give the device full bus interface capability.

Vendor D(Harris) and Vendor E(Raytheon) devices employ nichrome (Nicr) fuse technology. Devices from Vendors D and E are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position. Vendor F (Monolithic Memories Inc.) utilizes titanium-tungsten (TiW) fuse technology. Devices from Vendor F are manufactured storing a logical "0". Any bit can then be programmed for a logical "1".

Military grade DIP versions of the devices were received from the vendors for the characterization effort. Table 4.1 summarizes the manufacturer, quantity received, access time, part number, and date code.

Table 4.1 Devices Procured for Characterization

Vendor	Part No.	Access Time	Date Code	Quantity
D	HM-76321-2	85nS	8209	18
D	HM-76321-2	85nS	8251	15
E	R29671DMB	100nS	8304	25
F	5383281D	60nS	8301	15

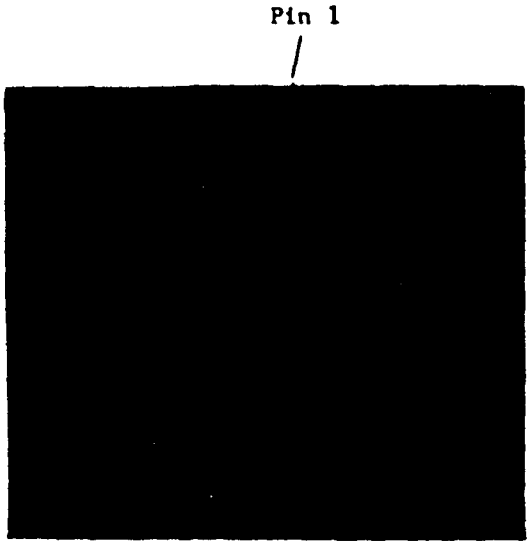
All Vendor D and E devices were received in an unprogrammed state. Vendor F devices were pre-programmed by the manufacturer.

Table 4.2 provides a comparison in chip dimensions for the two vendors. Photographs of a die from each vendor are in Figure 4.1. All photographs are to the same scale so that a visual size comparison can be made.

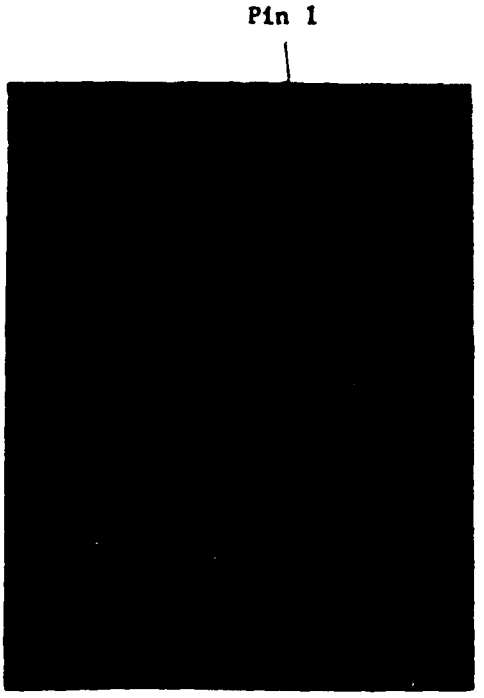
Table 4.2 32K FPROM Chip Dimensions

Vendor	Length (mm)	Width (mm)	Area (sq mm)
D	4.39	5.08	22.30
E	5.84	4.52	26.40
F	5.03	5.72	28.77

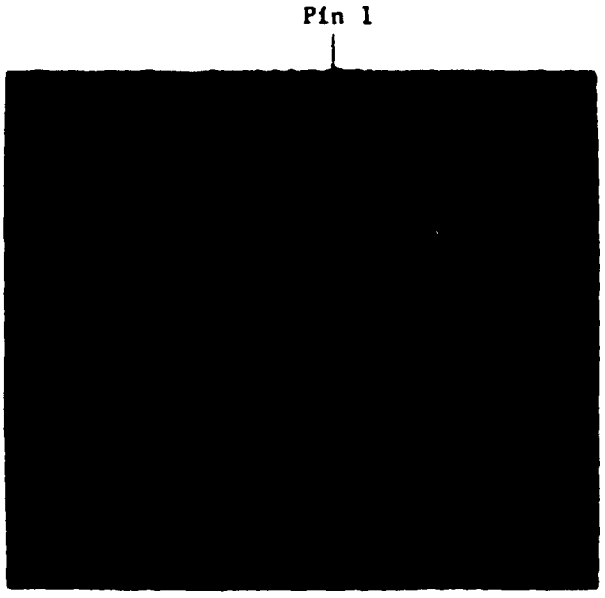
The devices provided for the characterization were packaged in 24 pin DIPs. Figure 4.2 displays the pin configuration which is the same for all three vendors.



Vendor D

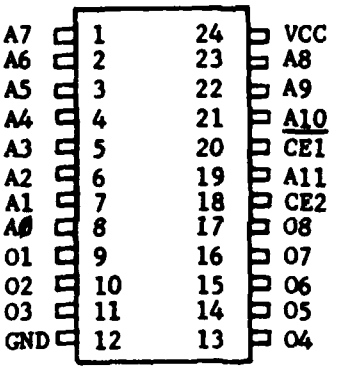


Vendor E



Vendor F

Figure 4.1 Die Photos - 4Kx8 FPROM (14.84X)



Vendor D, Vendor E, Vendor F

Figure 4.2 32K FPROM Pin Configuration

4.2 Incoming Tests

Devices from Vendors D and E were subjected to an incoming test to verify that all bits were in the unprogrammed state. In addition, the following DC parameters were tested to ensure device integrity before programming: ICC, IIH, IIL, IOHZ, IOLZ, VIC and VOH.

All devices procured from Vendors D and E passed the incoming test. Because the devices from Vendor F were received pre-programmed, they did not undergo an incoming test, but were immediately subjected to the DC characterization.

4.3 DC Parameters

DC Parameters were characterized using the methods described in section 2.3 and the individual sections that follow. DC Parameter testing was performed on sixteen devices from Vendors D and E and fifteen devices from Vendor F.

Table 4.3 lists the DC parameters and test conditions specified by each of the three vendors.

Table 4.3 Vendor Specified DC Parameters

Symbol	Parameter	Vendor D Min	Vendor D Max	Vendor E Min	Vendor E Max	Vendor F Min	Vendor F Max	Unit
ICC	Supply Current		190		195		190	mA
VCC	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
VIC	Input Clamp Voltage		-1.2 Iin=-18mA		-1.5 Iin=-18mA		-1.5 Iin=-18mA	V
IIL	Input Leakage Current		-100 VIL=0.45v		-250 VIL=0.4V		-250 VIL=0.4V	uA
IIH	Input Leakage Current		40 VIH=VCCMAX		100 VIH=VCCMAX		40 VIH=VCCMAX	uA
VIL	Low Level Input Voltage		+0.8	0	+0.8		+0.8	V
VIH	High Level Input Voltage	2.0		2.0	5.5V	2.0		V
IOLZ	Output Leakage Current		-40 VOL=0.3V		-100 VOL=0.45V		-40 VOL=0.4V	uA
IOHZ	Output Leakage Current		100		100		40	uA
VOL	Low Level Output Voltage		0.5 IOL=16mA		0.5 IOL=16mA		0.5 IOL=16mA	V
VOH	High Level Output Voltage	2.4 IOH=-2mA		2.4 IOH=-2mA		2.4 IOH=-2mA		V
IOS	Output Short Circuit Current	-15 VOUT=0V	-100	-12 VOUT=0.2V	-85	-20 VOUT=0V	-90	mA

4.3.1 Leakage Current

Input leakage currents, IIH and IIL, were measured at -55, 0, 25, 70, 110 and 125°C for the three vendors. No failures were detected and all measured currents were well below manufacturer specified limits.

Output leakage currents, IOHZ and IOLZ, were also measured at the six temperatures. All measurements of IOHZ and IOLZ were found to be well within manufacturer specified limits.

4.3.2 Logic Output Voltage (VOH, VOL)

All devices passed the specified VOH limit at 55, 0, 25, 70, 110 and 125°C. Figure 4.3 summarizes the average VOH values for each vendor under the same output current condition (-2.0mA). All vendors' devices exhibited a linear VOH, that increased slightly with temperature.

The specified VOL limit for all vendors is 0.5V at IOL = 16mA. However, Vendors D and F had previously indicated that the slash sheet specification should be 0.5V at IOL = 8mA. For this reason, all devices were characterized with IOL = 8mA. As Figure 4.3 illustrates, VOL values decreased linearly as temperature increased, with Vendor F exhibiting slightly lower values of VOL than Vendors D or E. Because the values of VOL for all vendors were well below 0.4V, this value was recommended as the specified VOL limit at IOL = 8mA in the preliminary slash sheet.

4.3.3 Input Threshold Voltage

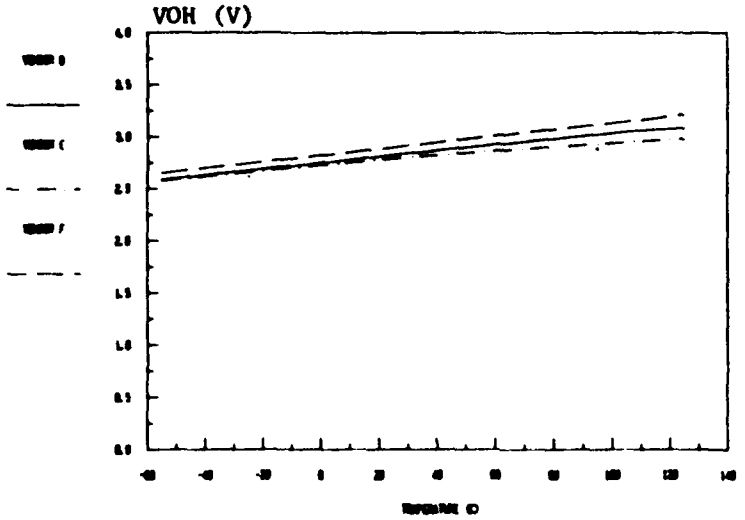
Threshold voltages(VIH and VIL) were measured on each input pin of every device using the methods described in section 2.3. Figure 4.4 summarizes the average input threshold voltages of each vendor over the military temperature range. The results are typical of bipolar devices, demonstrating a fairly stable linear response from each vendor.

The affects of input logic levels on output access times are discussed in the individual vendors' AC parameter section.

4.3.4 Supply Current (ICC)

The supply current measurements were performed at -55, 0, 25, 70, 110 and 125°C under the following conditions:

1) VCC = 5.5V
2) VIL = 0.0V applied to all inputs
3) Outputs open



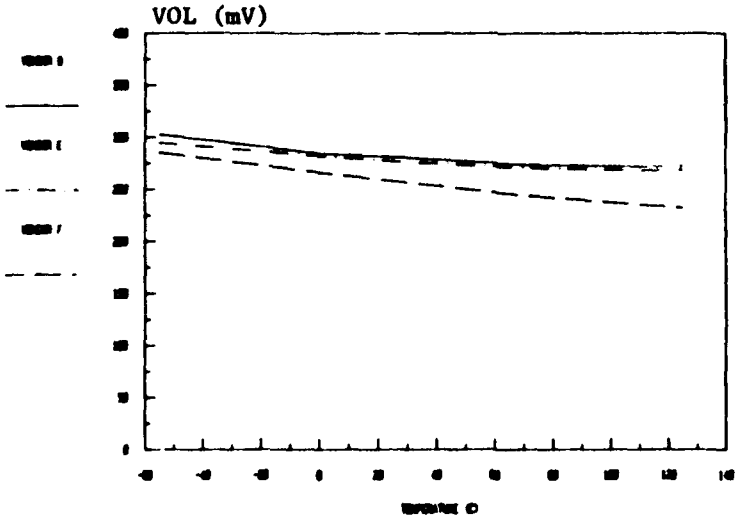
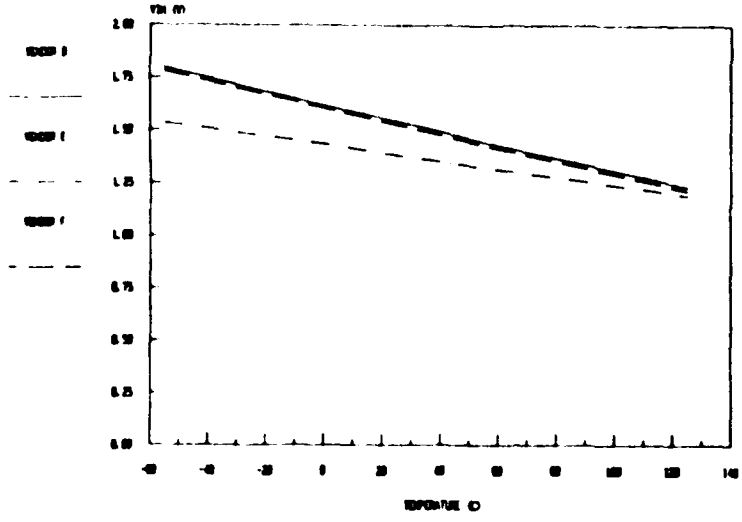


Figure 4.3 Average of VOH and VOL Values



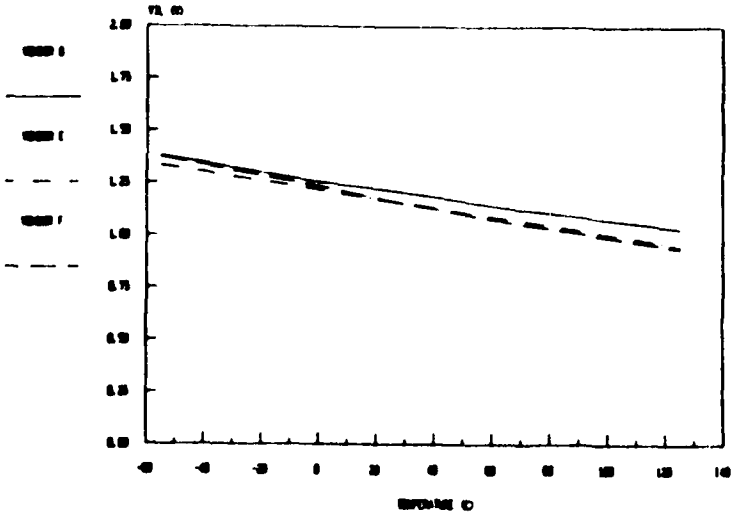


Figure 4.4 Average of VIH and VIL Values

Average values of ICC versus temperature are shown in Figure 4.5. As the plot indicates, all supply current measurements were well within vendor specified limits and are typical of bipolar devices over the military temperature range.

4.3.5 Input/Output Pin Capacitance

Capacitance measurements were performed on selected pins of six devices from each vendor. Table 4.4 lists the average minimum and average maximum measurement data. Vendor D was the only vendor to specify limits. Vendor D parts tend to have a lower capacitance per pin than Vendors E and F and fall within their maximum specified limits.

Table 4.4a Vendor D Avg. Min., Avg. Max. Pin Capacitance

Pin	Avg. Min.	Avg. Max.	Limit	Unit
A0-A11	6.0	8.6	8	pF
O1-O8	8.9	9.9	10	pF
CE1	5.0	5.1	8	pF
CE2	7.0	7.2	8	pF

Table 4.4b Vendor E Avg. Min., Avg. Max. Pin Capacitance

Pin	Avg. Min.	Avg. Max.	Limit	Unit
A0-A11	7.1	9.6	Not Available	pF
O1-O8	14.8	15.9	Not Available	pF
CE1	9.5	9.7	Not Available	pF
CE2	6.4	6.7	Not Available	pF

Table 4.4c Vendor F Avg. Min., Avg. Max. Pin Capacitance

Pin	Avg. Min.	Avg. Max.	Limit	Unit
A0-A11	6.4	11.9	Not Available	pF
O1-O8	8.6	9.6	Not Available	pF
CE1	9.3	9.6	Not Available	pF
CE2	15.5	16.0	Not Available	pF

4.3.6 Input Clamp Voltage (VIC)

Input clamp voltage test results exhibited a typically linear variation over the temperature range. Table 4.5, listing average input clamp voltage measurements at -55, 25 and 125°C, demonstrates this linearity. There were no VIC failures and all measured voltages were

well within manufacturer specified limits.

Table 4.5 Average Input Clamp Voltage

Vendor	-55°C	25°C	125°C	Units
D	603.4	489.4	380.9	mV
E	560.3	529.4	406.3	mV
F	445.0	383.0	283.5	mV

4.3.? Output Short Circuit Current (IOS)

Output short circuit current was measured over the entire temperature range with VCC = 5.5V. Figure 4.6 shows the average IOS for each vendor.

Devices from Vendors D and F experienced no failures and responded linearly over the temperature range. Although the average values of output short circuit current for Vendor F were 20mA to 40mA higher than Vendor D or Vendor E, these values were still well within the vendor's specified limit.

Vendor E exhibited linearity at lower temperatures, but a slight anomaly appears at the higher temperatures. Two devices exceeded the vendor's maximum limit of -85mA at 110°C and 125°C. However, at least one output on each device from Vendor E exhibited IOS values of less than -12mA at temperatures of 110°C and above. Repeated execution of IOS tests on the same devices resulted in erratic readings, sometimes passing well within the limits, sometimes failing with an IOS less than the minimum limit.

Discussions with Vendor E revealed that the upper transistor in the totem pole output occasionally turns off when 0V or a slightly negative voltage is applied. When the internal signal level feeding the output gate is close to the input threshold of the gate, the drive that turns on the upper transistor at the output is very weak. When 0V is applied for the IOS test, the drive to the upper transistor is degraded via the base-collector junction of the lower transistor. The degradation is such that the upper transistor is cut off or nearly cut off, thus reducing the short circuit current.

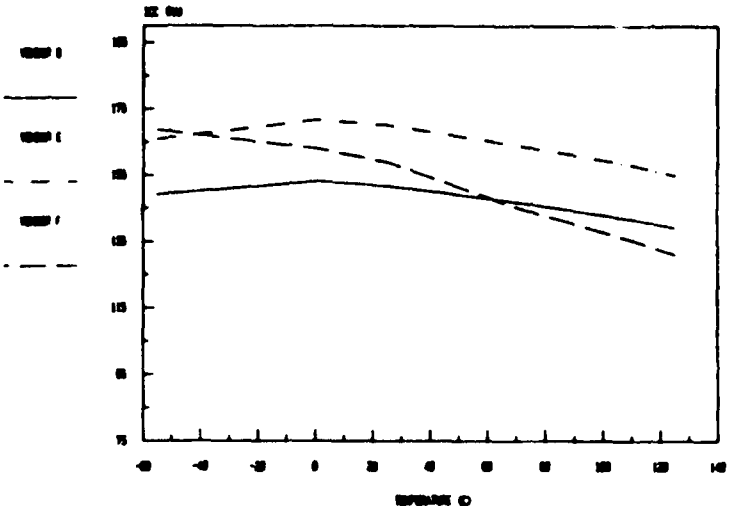


Figure 4.5 Average of ICC Values

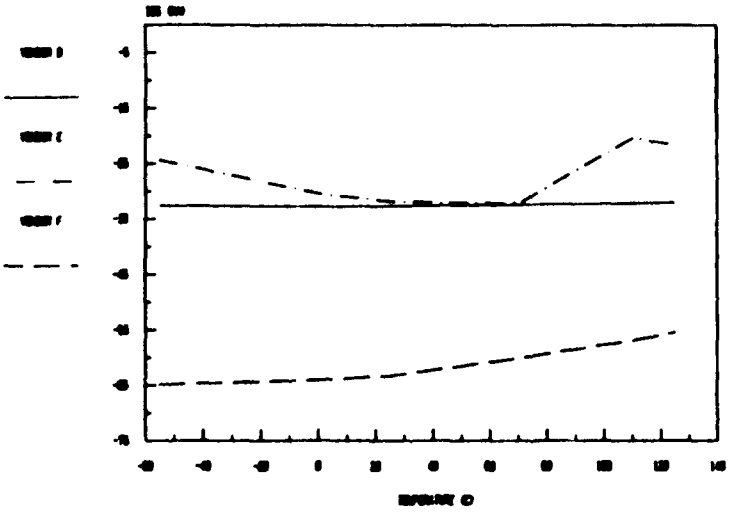


Figure 4.6 Average of IOS Values

4.4 AC Characterization

Timing parameters of each vendor were characterized under the following test conditions:

1) Temperature = -55, 0, 25, 70, 110, 125°C
2) VCC = 4.5V, 5.5V
3) VIH = 2.0V, VIL = 0.8V (case 1)
4) VIH = 2.4V, VIL = 0.6V (case 2)

All AC measurements discussed in this section were made using a binary search method with output compare levels of 2.4V and 0.8V. A 0.4V VOL compare level was initially used. However, it was determined that all three device types exhibited a perturbation on each output when transitioning to a logic low voltage. The perturbation, due to an impedance mismatch between the device output and the S-3270 tester, caused the output low level to momentarily rise above the 0.4V compare level before settling down to a steady state value. The test pattern used was a full address complement pattern. Table 4.6 lists the AC parameters that were characterized and the manufacturer specified limits. Refer to Appendix B for timing parameter abbreviations used in this section.

Table 4.6 Vendor Limits for AC Parameters

	Vendor D	Vendor E	Vendor F
TAVQV	85ns	100ns	60ns
TELQV	40ns	50ns	35ns
TEHQV	40ns	50ns	35ns

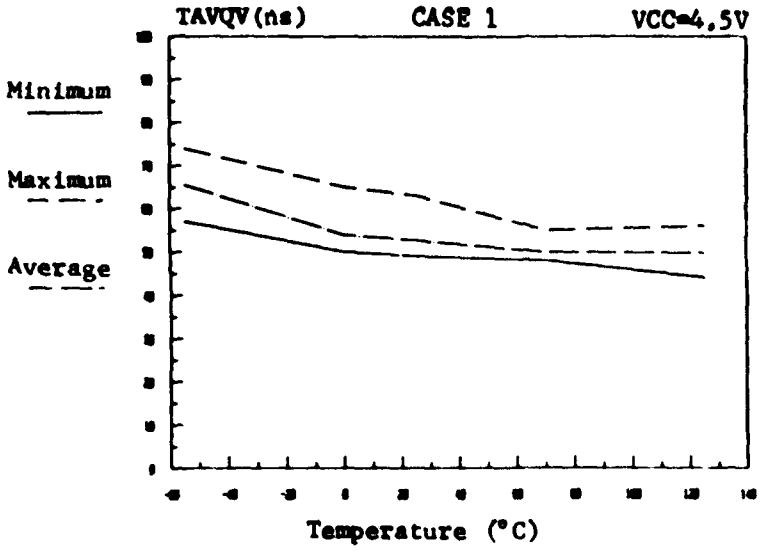
4.4.1 Vendor D AC Parameters

Sixteen devices from Vendor D were tested. All Vendor D devices were well within their specified limits for each parameter over the specified temperature range.

4.4.1.1 Address,Chip Enable 1,and Chip Enable 2 Access Times

Figure 4.7 summarizes the measured results of address access time (TAVQV) at VCC=4.5V and VCC=5.5V. Each set of three points at one temperature represents minimum(min), average(avg), and maximum(max) measured parameter values for sixteen devices.

The plots of (TAVQV) for both cases of VCC display similar trends.



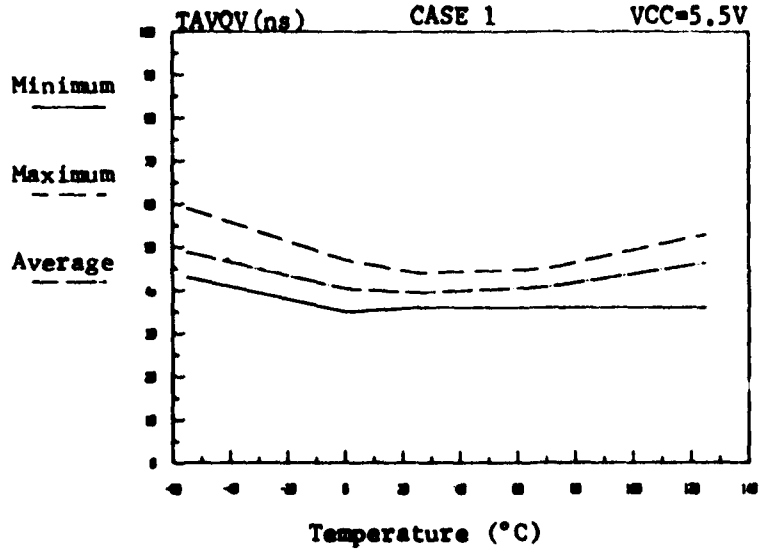


Figure 4.7 Vendor D - Address Access Time vs. Temperature for Case 1 Logic Levels

While decreasing slightly as temperature increased from -55°C to 25°C, access times were quite stable, varying only 10ns over the temperature range at both VCC=4.5V and VCC=5.5V. Access times were approximately 15ns faster at the higher VCC, but all measurements were within the specified limit of 85ns.

Both plots of Figure 4.7 are for case 1 logic levels. Plots of TAVQV for case 2 logic levels were omitted due to their similarity to case 1.

Chip enable access times are plotted in Figure 4.8(TELQV) and Figure 4.9(TEHQV). Once again, case 2 plots are omitted due to their similarity to case 1.

As with address access time measurements on these devices, chip enable access times (both TELQV and TEHQV) exhibit little sensitivity to temperature change. As little as 10ns variation is seen when temperature is increased from -55°C to 125°C. A 10ns to 15ns decrease in both TELQV and TEHQV is noted as VCC is increased from 4.5V to 5.5V.

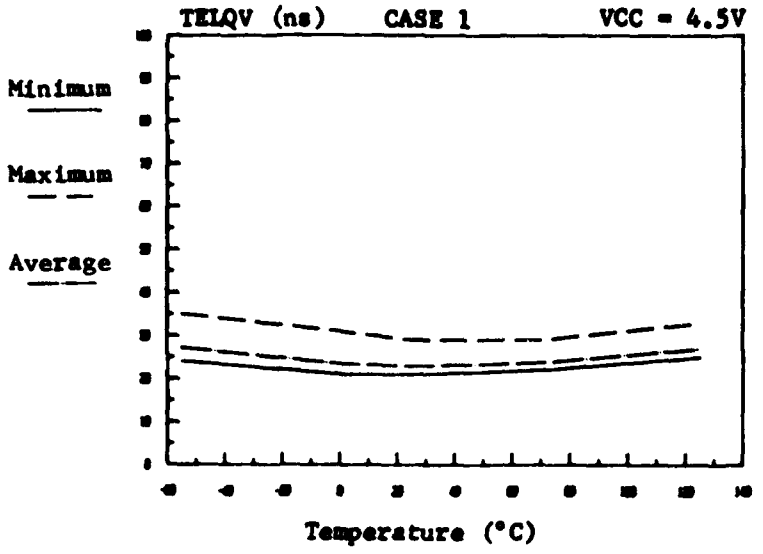
4.4.2 Vendor E AC Parameters

Sixteen devices from Vendor E were tested under the conditions described in Section 4.4. While no address access time failures occurred during testing, chip enable access time failures were common to all the devices.

4.4.2.1 Address,Chip Enable 1,and Chip Enable 2 Access Times

Figure 4.10 displays the summarized results of address access time (TAVQV) measurements at VCC=4.5V and VCC=5.5V for case 1 logic levels. At these access times at both VCC's exhibit similar trends. TAVQV decreases as the temperature increases from -55°C to 0°C, then increases with temperature from 0°C to 125°C. Despite this slight increase in TAVQV, all devices from Vendor E were well within the Vendor specified limit of 100ns when tested at both values of VCC and case 1 logic levels.

Address access time results for case 2 logic levels at VCC=4.5V are shown in Figure 4.11. Once again, all devices were well within Vendor's limits, with very little variance in access time (less than 15ns) over the military temperature range. Due to its similarity to case 2 at VCC=4.5V, a plot of case 2 at VCC=5.5V is omitted.



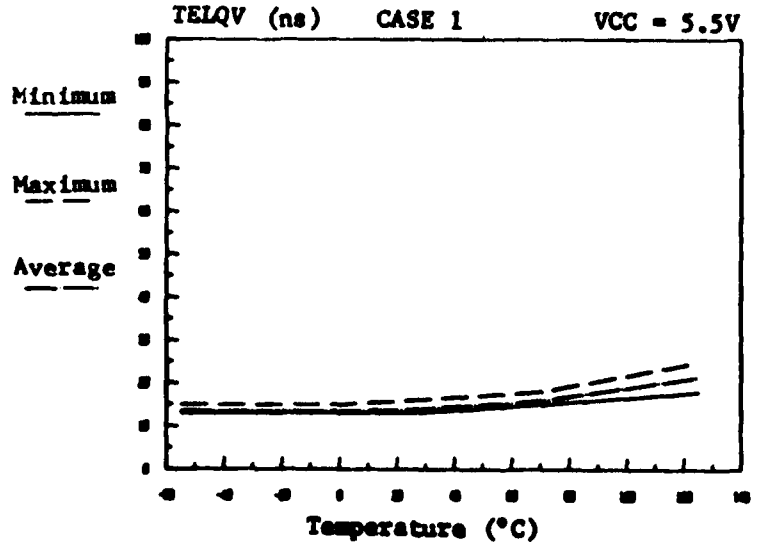
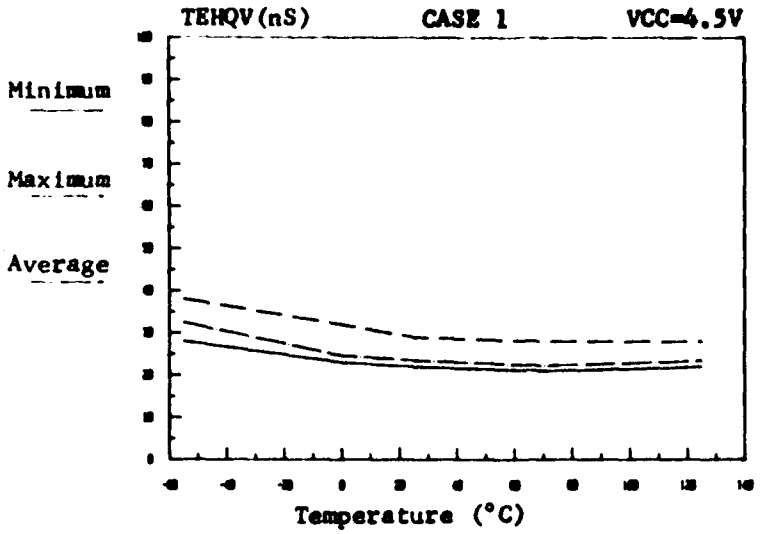


Figure 4.8 Vendor D - Chip Enable 1 Access Time vs. Temperature for Case 1 Logic Levels



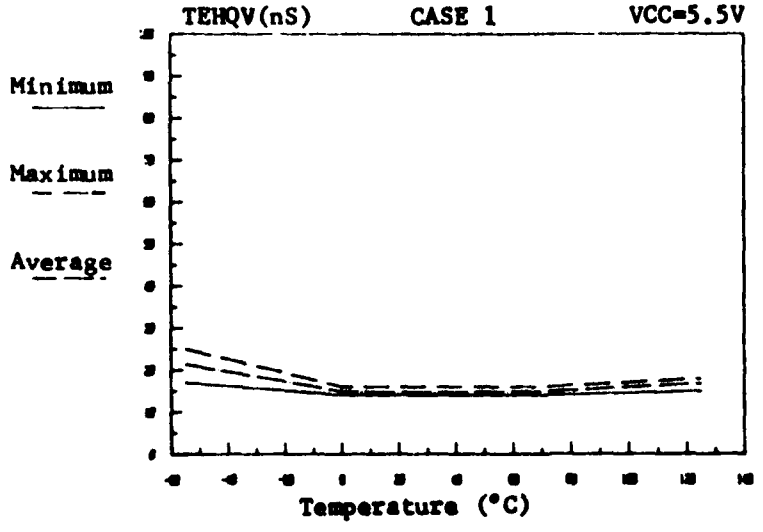
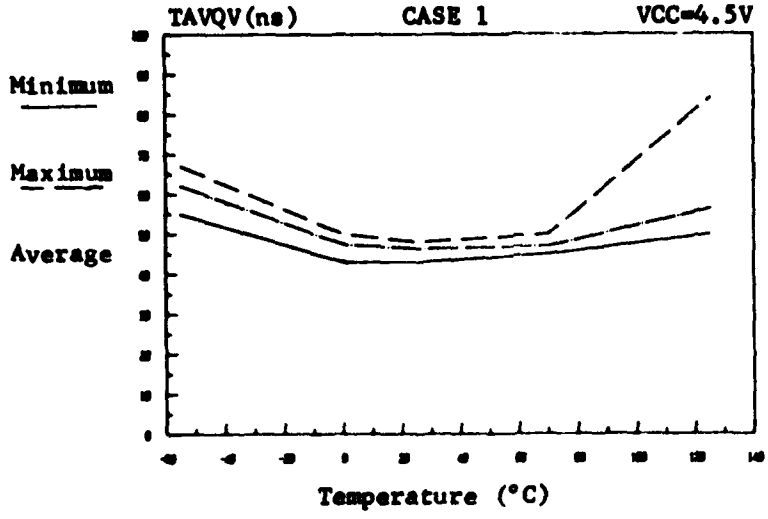


Figure 4.9 Vendor D - Chip Enable 2 Access Time vs. Temperature for Case 1 Logic Levels



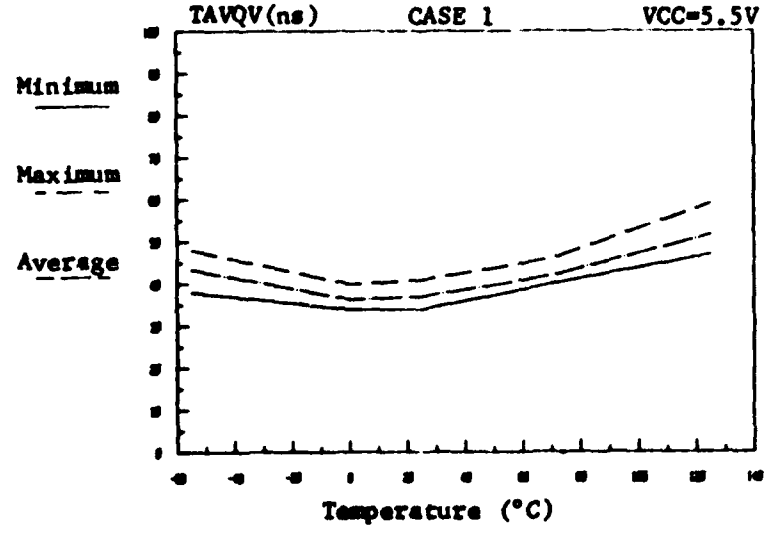


Figure 4.10 Vendor E - Address Access Time vs. Temperature for Case 1 Logic Levels

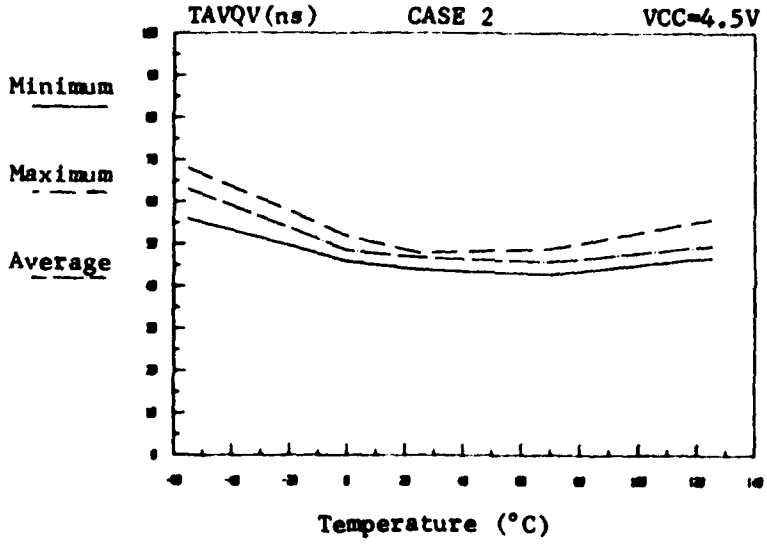


Figure 4.11 Vendor E - Address Access Time vs. Temperature for Case 2 Logic Levels

Figures 4.12 and 4.13 summarize chip enable access times, TELQV and TEHQV, at two VCC levels and both cases of logic levels. Both parameters exhibit almost identical trends with respect to the test conditions. Therefore, the following analysis applies to both TELQV and TEHQV.

All Vendor E devices experienced chip enable access time failures with VCC=4.5V at case 1 logic levels. As Figures 4.12 and 4.13 illustrate, the average values of TELQV and TEHQV exceed the Vendor's limit of 50ns by 5ns to 15ns. However, when VCC is raised to 5.5V, access times at -55°C to 25°C are reduced 20ns to 30ns. Above 25°C access times again increase with temperature. Five devices failed TELQV at 125°C, but the average values of both TELQV and TEHQV are 20ns to 30ns less at VCC=5.5V.

When case 2 logic levels are employed (Figures 4.14 and 4.15), the results are similar to case 1. All devices experienced failures at the lower VCC, particularly at lower temperatures. However, all devices were well within the Vendor's limits when VCC is raised to 5.5V. Also, case 2 logic levels appear to stabilize the access times with respect to temperature. Very little change in TELQV and TEHQV is noted when case 2 levels are applied.

In summary, supply voltage significantly affects chip enable access times. Lower values of VCC result in access times which exceed the manufacturer's limit regardless of logic levels. The logic levels themselves, however, do impact access time measurements. A sensitivity to higher temperatures appears when case 1 logic levels are used resulting in higher access times at high temperature.

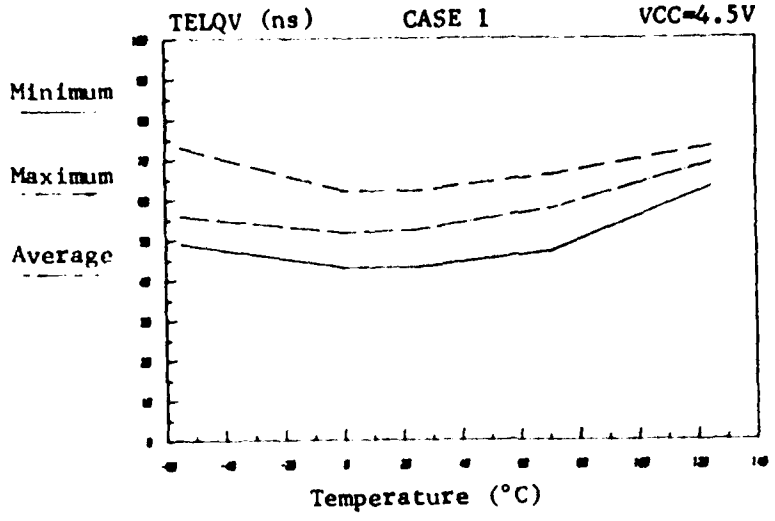
4.4.3 Vendor F AC Parameters

AC parametric testing was performed on fifteen devices from Vendor F under the conditions described in Section 4.4. Several devices experienced address access time and chip enable access time failures.

4.4.3.1 Address,Chip Enable 1,and Chip Enable 2 Access Times

Eight devices failed to meet the Vendor's limits for both address access time (TAVQV) and chip enable 1 access time (TELQV) at -55°C.

Figures 4.16 and 4.17 summarize TAVQV measurements. The plots indicate a sensitivity to case 1 logic levels at the temperature extremes. Eight devices failed at -55°C with VCC=4.5V and case 1 logic levels. Under these same conditions, only one device failed TAVQV at 125°C. When VCC was raised to 5.5V, all devices passed, but access times at -55°C and 125°C were still 10ns to 15ns slower than those at 25°C.



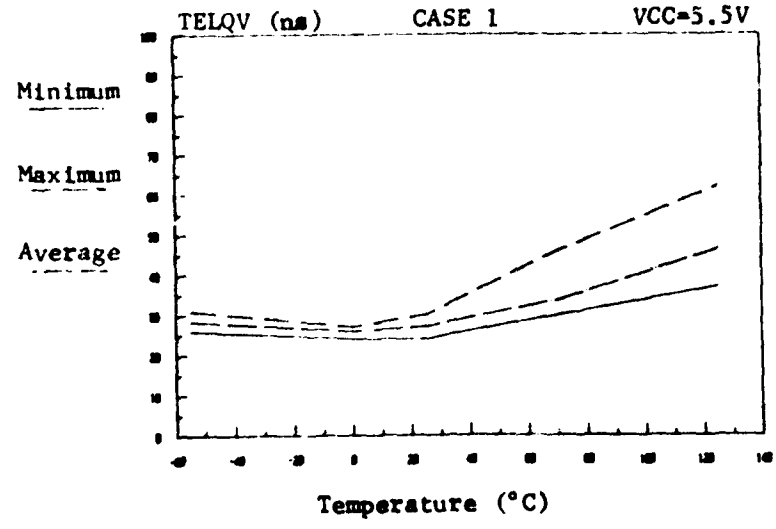
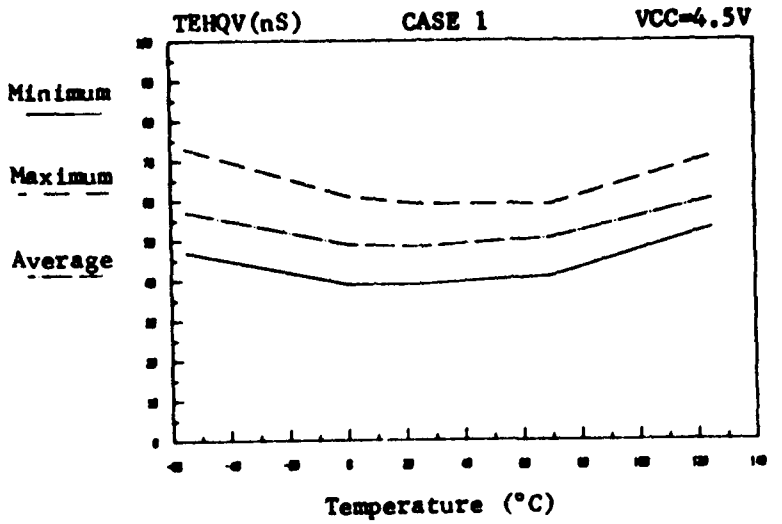


Figure 4.12 Vendor E - Chip Enable 1 Access Time vs. Temperature for Case 1 Logic Levels



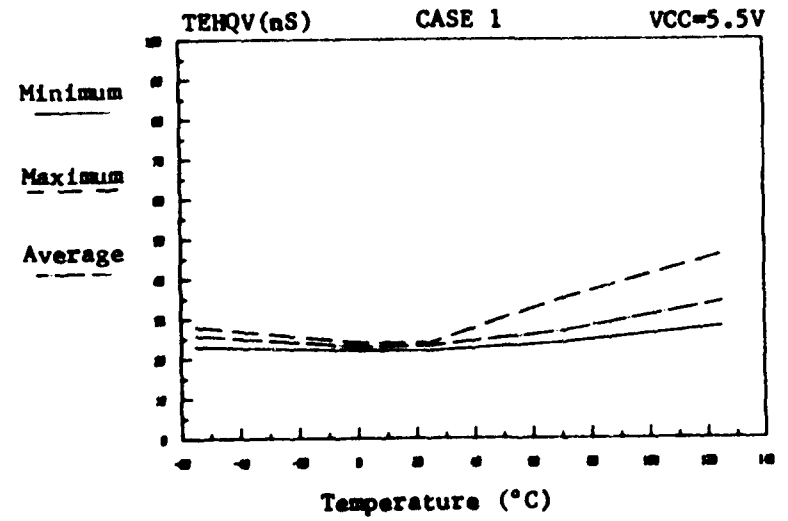
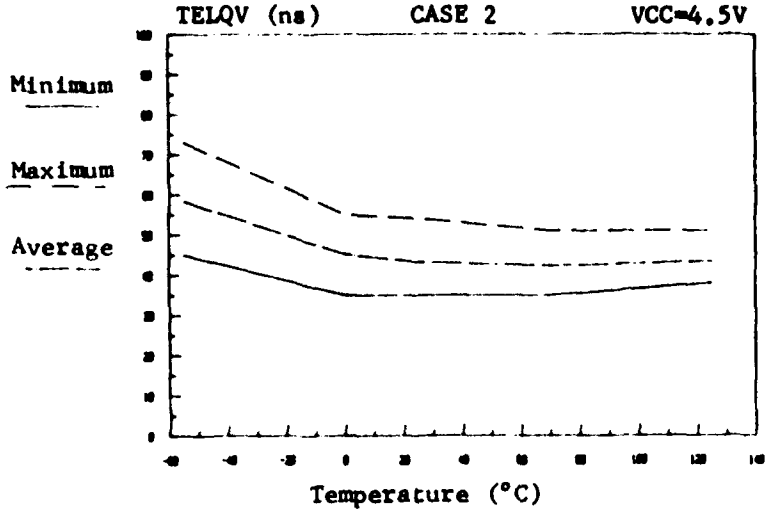


Figure 4.13 Vendor E - Chip Enable 2 Access Time vs. Temperature for Case 1 Logic Levels



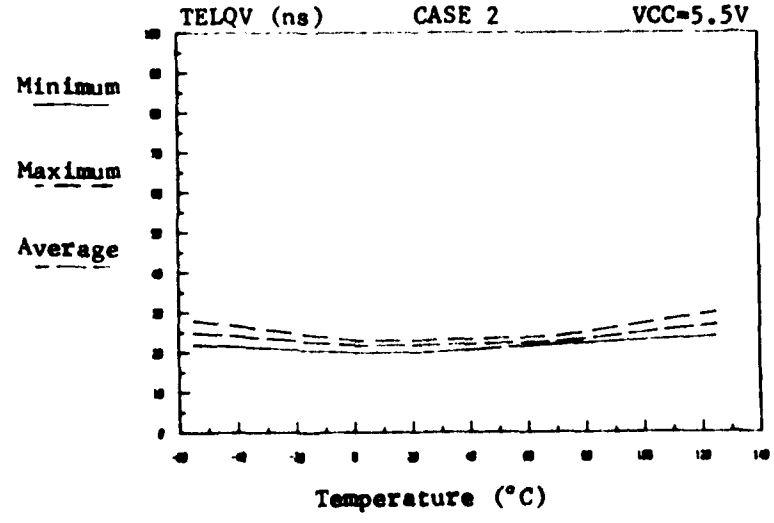
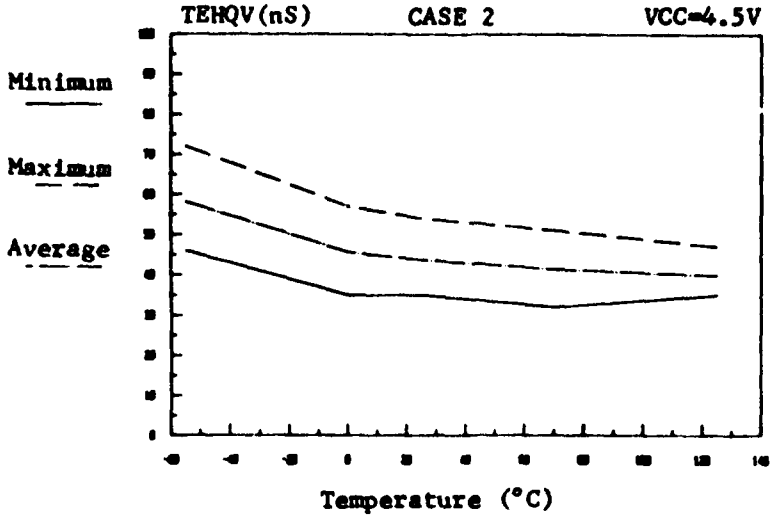


Figure 4.14 Vendor E - Chip Enable 1 Access Time vs. Temperature for Case 2 Logic Levels



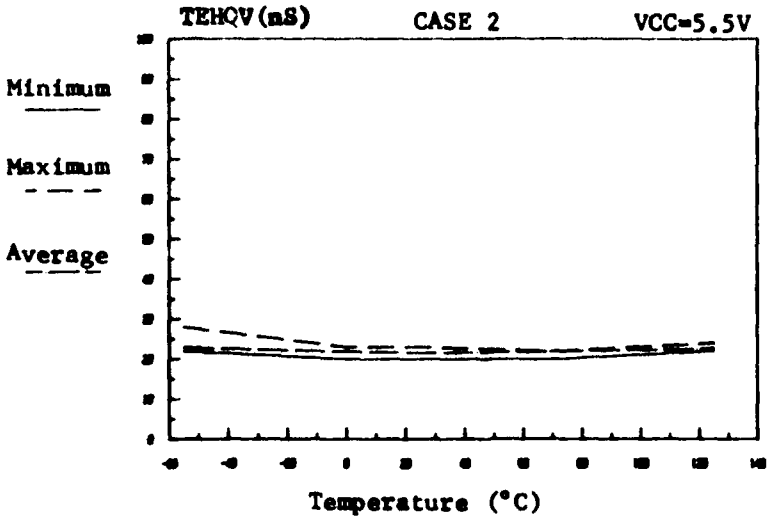
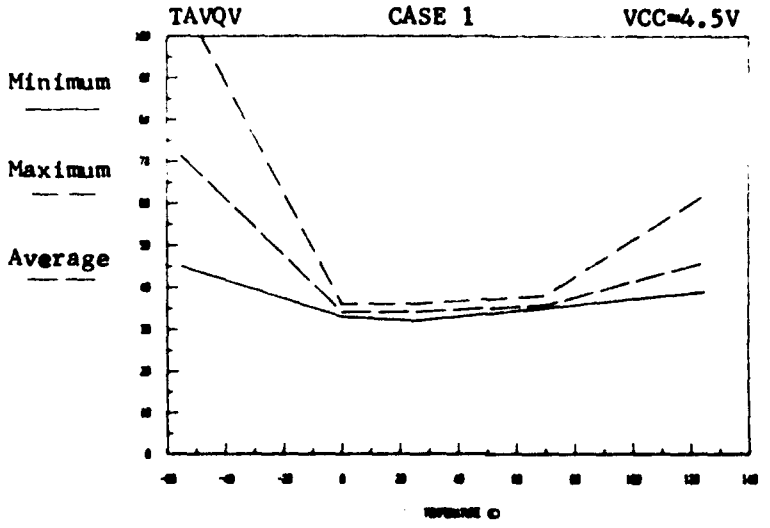


Figure 4.15 Vendor E - Chip Enable 2 Access Time vs. Temperature for Case 2 Logic Levels



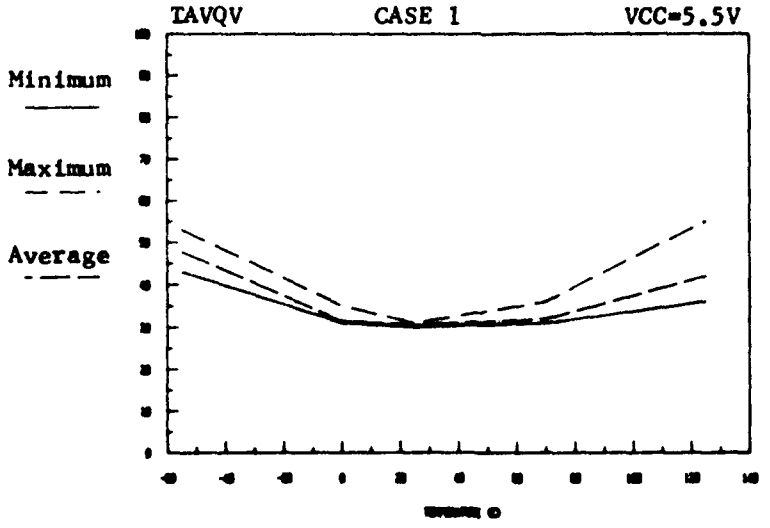
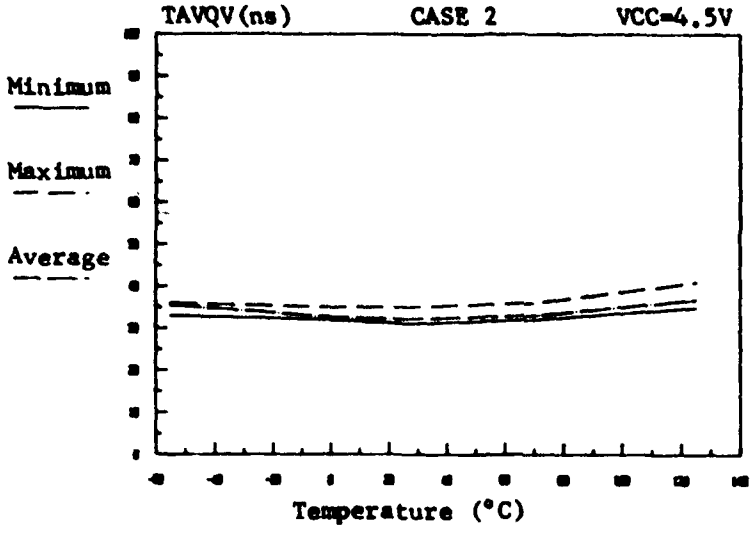


Figure 4.16 Vendor F - Address Access Time vs. Temperature for Case 1 Logic Levels



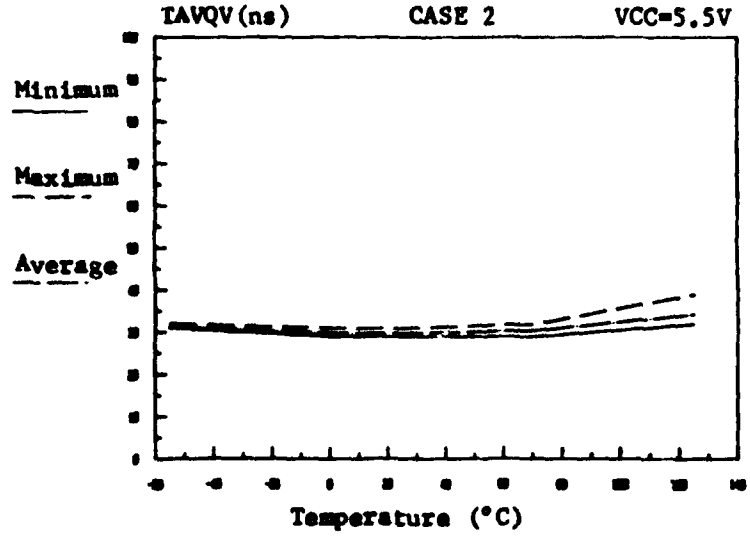


Figure 4.17 Vendor F - Address Access Time vs. Temperature for Case 2 Logic Levels

When case 2 logic levels were employed, however, all fifteen devices demonstrated very little sensitivity to temperature variance and access times were well below the Vendor limit of 60ns.

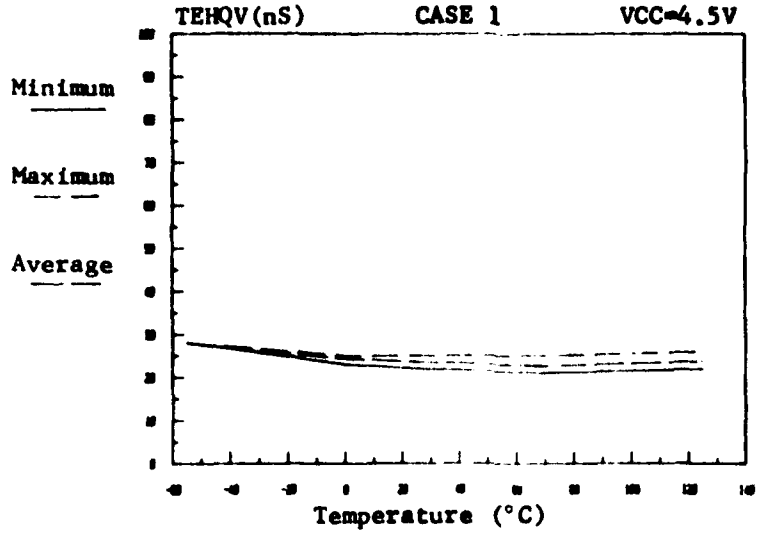
All Vendor F devices also passed chip enable 2 access time (TEHQV) testing. As the tight grouping of the minimum, average, and maximum plots in Figure 4.18 indicate, TEHQV varies little from device to device across the entire military temperature range at both supply voltage levels at case 1 logic levels. Results for case 2 logic levels were similar.

Measurement of chip enable 1 access times revealed a sensitivity to input logic levels similar to that which affected address access time. In this case (see Figure 4.19), eight devices yielded TELQV times greater than the Vendor's limit of 35ns. These failures all occurred at -55°C when VCC=5.5V and case 1 logic levels were used. Reducing the supply voltage to 4.5V resulted in all devices falling well within manufacturer specified limits. The use of case 2 logic levels also resulted in extremely stable access times across the entire temperature range at both levels of VCC. Figure 4.20 displays TELQV results for case 2 at VCC=5.5V. Case 2 plots of TELQV when VCC=4.5V are omitted due to their similarity to case 2 at VCC=5.5V.

4.4.4 Output Disable Time (TOHQZ)

Output disable time data was taken using both methods described in Section 2.4.2.2. Six devices from each vendor were tested. Although slight differences in disable time measurements were noted between the two methods, these differences were consistent from device to device from each vendor and all values were within the particular vendor's specified limits.

Tables 4.7a and 4.7b list average disable times, vendor and method of measurement employed.



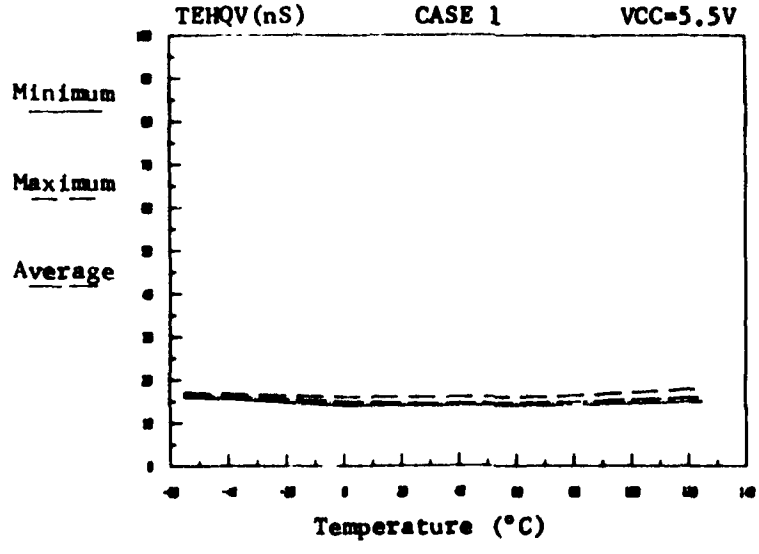
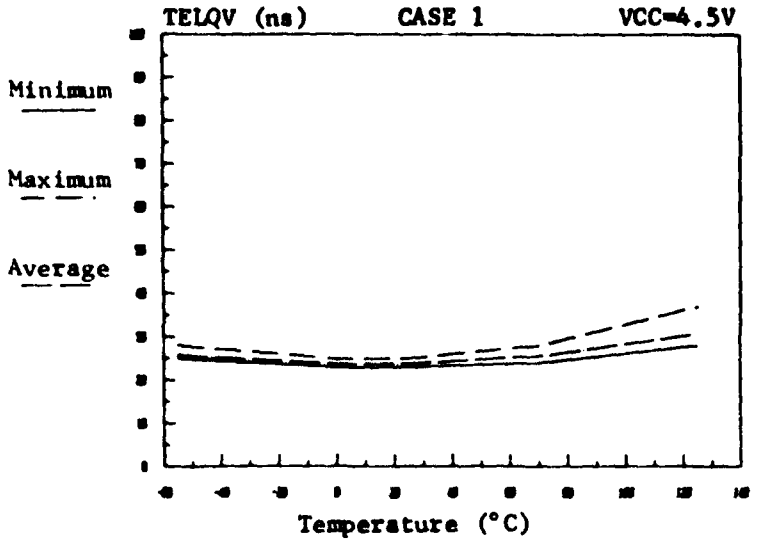


Figure 4.18 Vendor F - Chip Enable 2 Access Time vs. Temperature for Case 1 Logic Levels



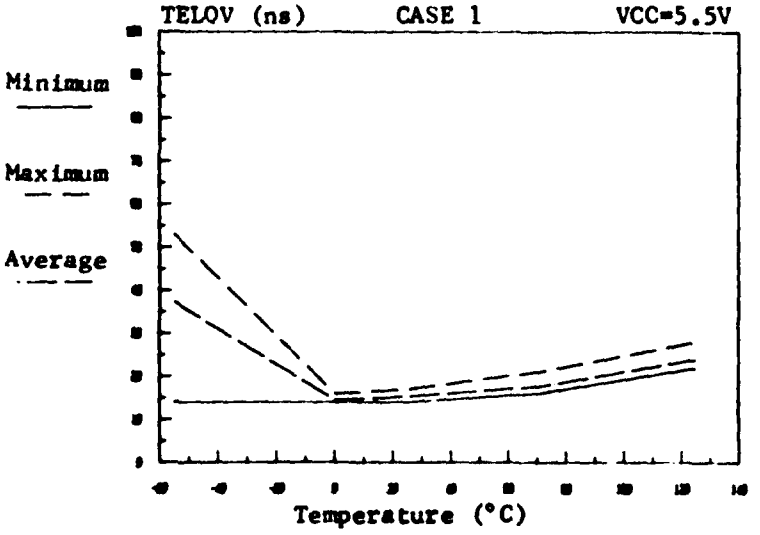


Figure 4.19 Vendor F - Chip Enable 1 Access Time vs. Temperature for Case 1 Logic Levels

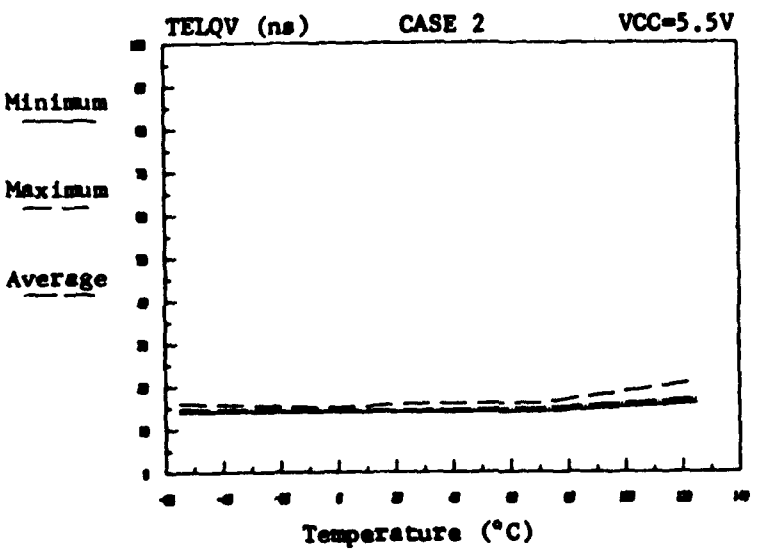


Figure 4.20 Vendor F - Chip Enable 1 Access Time vs. Temperature for Case 2 Logic Levels

Table 4.7a Output Disable Time - Output initially at VOH

Vendor	Average Disable Time (Zero Current)	(-0.5V)	Units
D	18.5	23.7	nsec
E	18.5	24.7	nsec
F	19.0	24.3	nsec

Table 4.7b Output Disable Time - Output initially at VOL

Vendor	Average Disable Time (Zero Current)	(+0.5V)	Units
D	35.0	27.5	nsec
E	27.2	23.5	nsec
F	25.2	22.3	nsec

4.4.5 AC Characterization Summary

Each vendor was tested under identical conditions. Vendor D was the only vendor of the three whose devices were able to meet their own specified limits for each AC parameter over all conditions. Vendor E exhibited sensitivity to supply voltage levels, while Vendor F was sensitive to input logic levels at the military temperature extremes.

In general, the address access times exhibited by Vendor F devices were faster than Vendors D and E. However, eight devices from Vendor F failed to meet the vendor's specified limit at -55°C, 4.5V and case 1 logic levels.

Chip enable 1 access times of Vendor E were greater than those of both Vendors D and F. All Vendor E devices exceeded the vendor's limit at 4.5V. Eight devices from Vendor F failed at -55°C, 5.5V and case 1 logic levels.

The chip enable 2 access times of Vendors D and F were also faster than those of Vendor E. All Vendor E devices again exceeded the vendor limit at 4.5V.

Output disable time measurements for each vendor exhibited no significant differences between vendors. All TOHQX values were within the vendor's specifications.

4.5 Pattern Sensitivity

March, Row/Column Complement and Gallop test patterns were applied to six devices from each vendor at 25°C to determine their address access time sensitivity at VCCs of 4.5 and 5.5 volts. The following cases of logic levels were used in this test.

CASE 1: VIH = 2.0V, VIL = 0.8V
CASE 2: VIH = 2.4V, VIL = 0.6V

Table 4.8 displays worst case access times for the three test patterns at each set of logic levels. Each value in the table represents an average access time of the six devices from each vendor. From the table there is no appreciable change in access time values from one pattern to another. In each case, the access time for the Gallop pattern is slightly higher than the March or Row/Column Complement values. To isolate an access time limit using the March and Row/Column Complement test required approximately 3-5 seconds. The Gallop test required up to 5 minutes to isolate a limit. The Gallop test has frequently been considered worst case since a transition occurs between every possible pair of addresses. The Row/Column Complement test generates more decoder activity per cycle than the March test and requires significantly less execution time than the Gallop test. For this reason, Row/Column Complement test patterns are recommended for the slash sheet.

No appreciable change in TAVQV for Vendor D, E, or F was observed between logic levels. Vendor F displayed no appreciable change in access time due to increasing VCC from 4.5 to 5.5V. Vendor D and E access times were 10 to 15 ns greater for VCC = 4.5V.

Table 4.8 Pattern Sensitivity Result Summary

Vendor D	TAVQV, CASE 1		TAVQV, CASE 2	
	VCC=4.5V	VCC=5.5V	VCC=4.5V	VCC=5.5V
March	52.7	43	52	42
Row/Column Complement	52.5	41.9	52	41.6
Gallop	52.8	43.2	52.2	42.3

Vendor E	TAVQV, CASE 1		TAVQV, CASE 2	
	VCC=4.5V	VCC=5.5V	VCC=4.5V	VCC=5.5V
March	60.2	46.8	61.8	46.7
Row/Column Complement	59.4	42.3	60.6	46.4
Gallop	61	47.8	61.9	47

Vendor F	TAVQV, CASE 1		TAVQV, CASE 2	
	VCC=4.5V	VCC=5.5V	VCC=4.5V	VCC=5.5V
March	36.2	33.2	35.5	32.7
Row/Column Complement	36.2	33.1	35.7	32.9
Gallop	37.2	33.8	35.8	33.6

4.6 Programming Parameters

Testing of selected programming parameters was performed on six devices from both Vendor D and Vendor E at 25°C. Devices from Vendor F were pre-programmed by the manufacturer, therefore characterization of programming parameters was not performed on these parts.

Programming parameter testing consisted of fixing the parameter to be tested at a value that would verify the manufacturer's limits. This was performed while keeping the other programming parameters at a nominal value. A block of 128 byte locations was then programmed and verified.

4.6.1 Vendor D Programming Parameters

Vendor D programming parameters and the values they were verified at are as follows:

1. Output Enable Voltage During Programming (VOPE) 8.5V, 10.5V, 12.5V
2. Output Enable Voltage Pulse Width (TP) 70uS, 100uS, 120uS
3. Voltage to VCC During Programming (VPH) 10.0V, 12.0V, 13.0V

Table 4.9 lists the manufacturer's specified limits of the programming parameters that were characterized.

Table 4.9 Vendor D Specified Limits for Programming Parameters

Parameters	Minimum	Maximum	Units
VOPE	10.5	11.0	V
TP	90.0	110.0	uS
VPH	12.0	12.5	V

All six devices from Vendor D were programmed and verified at the indicated parameter test values. Reducing VOPE below 8.5V or VPH less than 10.0V resulted in numerous programming failures. Pulse width (TP) has little affect on programmability as TP was reduced to as little as 10uS with no failures.

4.6.2 Vendor E Programming Parameters

Vendor E programming parameters and the values they were verified at are as follows:

1. Programming Voltage on Output Pin (VOUT) 16V, 20V, 30V
2. Programming Voltage on Programming Pin (VPP) 24V, 27V, 35V
3. Output Pin Programming Voltage Pulse Width (TP) 0.1uS, 30uS, 64uS
4. VCC During Programming (VCC) 4.2V, 4.5V, 5.5V

Table 4.10 lists the vendor's specified limits for the programming parameters that were tested.

Table 4.10 Vendor E Specified Limits For Programming Parameters

Parameter	Minimum	Maximum	Units
VOUT	20	26	V
VPP	27	33	V
TP	1	40	uS
VCC	5.4	5.6	V

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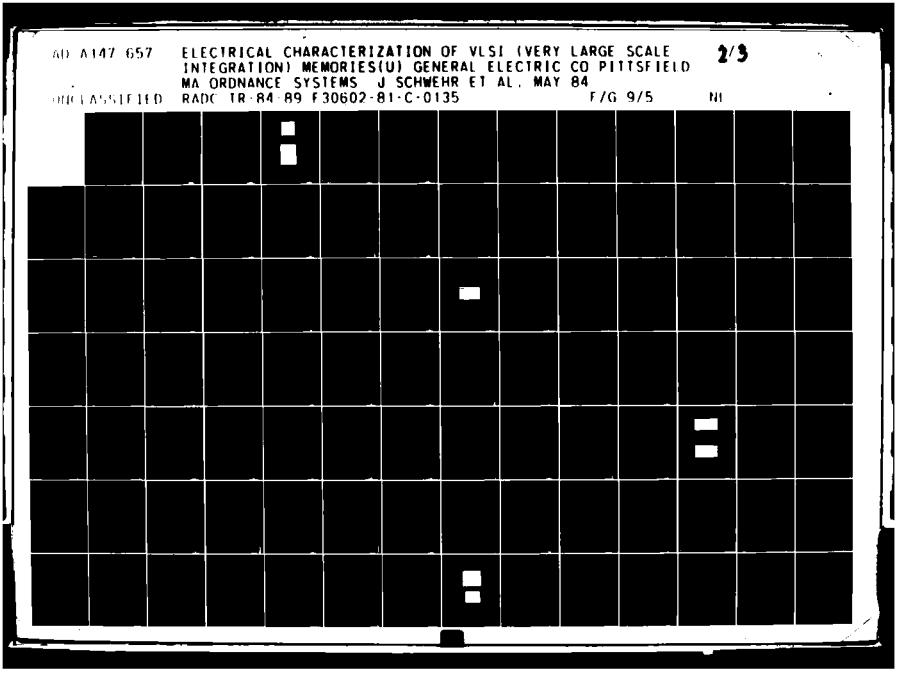
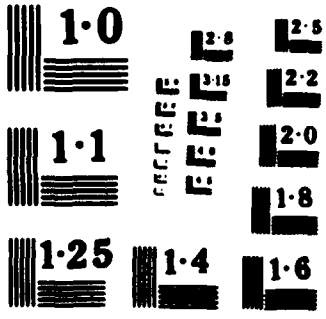
UNCLASSIFIED RADC-TR-84-89 F30602-81-C-0135 F/G 9/5 NL




1·0
1·1
1·25
1·4
2·5
2·2
2·0
1·8
1·6

All six devices from Vendor E programmed and verified normally at the indicated test values. Supply voltage level and pulse width had no affect on programmability. Reducing VOUT to less than 16V or decreasing VPP below 24V resulted in numerous programming failures.

4.7 Burn-In

All devices from each vendor were subjected to a dynamic burn-in at 125°C for 160 hours. Each device was then retested(AC and DC) at 25°C. One device from Vendor D suffered a functional failure associated with several addresses. All other devices from each vendor were unaffected by the burn-in.

5. 64K UV-EPROM

5.1 Introduction

The 2764 UV-EPROM (ultraviolet erasable PROM) is a 65,536 bit static N-channel MOS erasable and reprogrammable read only memory. Special features include separate output (OE) and chip enable (CE) control lines and single +5V operation in the read mode. One other supply (+21V) is needed for programming.

Each device utilizes a transparent quartz lid which allows ultraviolet erasure. The eight tri-state data outputs allow connection of several devices to a standard microprocessor bus. All inputs can be driven by standard TTL circuits without the use of external pull-up resistors, and each output can drive one standard TTL circuit without external resistors.

Commercial grade devices were procured from two vendors for the characterization effort. Vendor A refers to the Intel Corporation and Vendor G is a Japanese vendor, Fujitsu. The Fujitsu parts were provided to RADC by the vendor and were characterized to help assess the technology and perhaps make some comparison to the Intel part. Table 5.1 summarizes the quantities of devices received, date code and specified worst case access times.

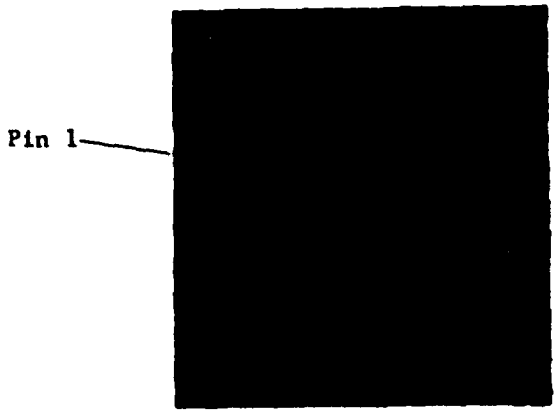
Table 5.1 Devices Procured For Characterization

Vendor	Part No.	Access Time	Date Code	Quantity
A	MD2764-451B	450	8220	20
A	MD2764-451B	450	8225	10
G	MBM2764-25	250	8149	25

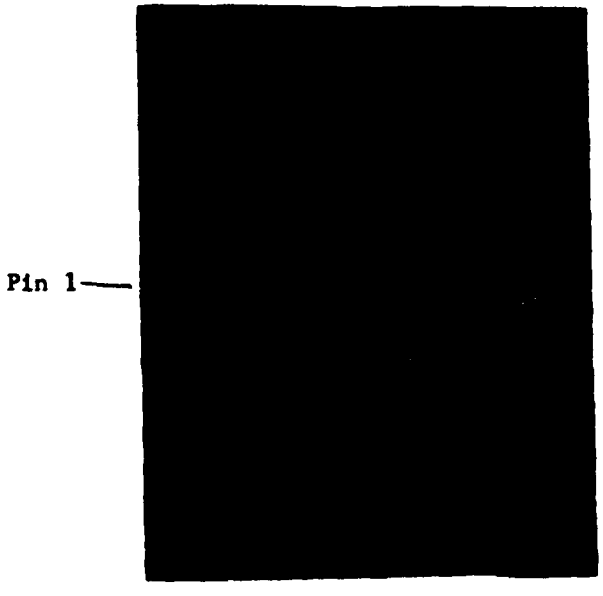
Table 5.2 provides a comparison in chip dimensions for the two vendors. Photographs of a chip from each vendor are in Figure 5.1. Both photographs are to the same scale so that a visual size comparison can be made.

Table 5.2 64K UV-EPROM Chip Dimensions

Vendor	Length (mm)	Width (mm)	Area (sq. mm)
A	3.63	3.91	14.19
G	4.32	5.51	23.80



Vendor A



Vendor G

Figure 5.1 Die Photos - 8Kx8 UV-EPROM (14.84X)

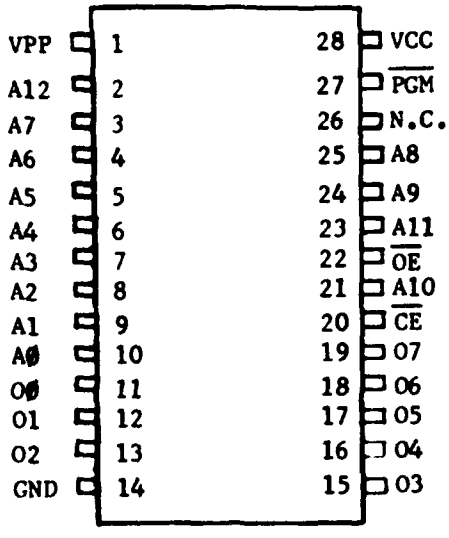
The devices provided for the characterization were packaged in 28 pin ceramic DIPS. Figure 5.2 displays the pin configuration for each vendor.

5.2 Incoming Tests

The incoming test verified the integrity of each bit by programming and erasing the devices with checkerboard and inverse checkerboard patterns. Six of the 30 devices from Vendor A did not pass the incoming test. The devices from Vendor G exhibited no incoming failures.

5.3 DC Parameters

Table 5.3 lists the DC parameters and test conditions specified by each of the two vendors. For the DC characterization the vendor specified conditions were applied, except during the supply current measurements. Both vendors specify a 5.25V maximum supply voltage limit. Since the slash sheet will specify a VCC range of 4.5V to 5.5V, the characterization applied 5.5V to all devices during the supply current measurements. The DC Parameters were measured at -55, 0, 25, 70, 100 and 125°C.



Vendor A, Vendor G

Figure 5.2 64K UV-EPROM Pin Configuration

Table 5.3 Vendor Specified DC Parameters

Symbol	Parameter	Vendor A Min	Vendor A Max	Vendor G Min	Vendor G Max	Units
VCC	Supply Voltage	4.75	5.25	4.75	5.25	V
ICC1	Supply Current (Standby)		40		35	mA
ICC2	Supply Current (Active)		100		150	mA
IPP1	VPP Supply Current (Read)		5		15	mA
IIL,IIH	Input Leakage Current		10		10	uA
IOLZ, IOHZ	Output Leakage Current		10		10	uA
VIL	Low Level Input Voltage	-0.1	+0.8	-0.1	+0.8	V
VIH	High Level Input Voltage	2.0	VCC+1	2.0	VCC+1	V
VOL	Low Level Output Voltage		0.45 IOL=2.1mA		0.45 IOL=2.1mA	V
VOH	High Level Output Voltage	2.4 IOH=-400uA		2.4 IOH=-400uA		V

5.3.1 Leakage Current

No leakage current failures were found and all measured currents were well below the manufacturer's specified maximum limit of 10uA.

Output leakage currents were also within the manufacturer's specified limit of 10uA.

5.3.2 Logic Output Voltage (VOH, VOL)

All devices passed their specified VOH limit. The VOH results were summarized by finding the minimum VOH for each device (eight VOH values per device) and taking the average of the minimums over all the devices.

The average minimum VOH values versus temperature for both vendors are plotted in Figure 5.3a. Since both vendors specify the same output current condition (IOH) of 400uA, the plot gives a good indication of the difference in minimum VOH values. According to the plot, Vendor A values are slightly lower than Vendor G values.

As with VOH, all devices passed the vendor specified VOL limits at all temperatures. In summarizing values for VOL, the maximum value for each device is used to calculate an average that is plotted for each vendor in Figure 5.3b. Since IOL for both vendors is 2.1mA, the plot in Figure 5.3b allows a comparison of VOL values for both vendors. The plot shows Vendor G values were significantly higher than Vendor A values, but well within specifications.

5.3.3 Input Logic Level Sensitivity

Two devices from both vendors were subjected to worst case access time measurements to determine their sensitivity to various input logic levels. Three different sets of input conditions were used; they are as follows:

CASE 1: VIL = 0.4V, VIH = 3.0V

CASE 2: VIL = 0.6V, VIH = 2.4V

CASE 3: VIL = 0.8V, VIH = 2.0V

While varying input voltage levels, measurements were made of access time at 25°C with VCC levels of 4.5V, 5.0V, and 5.5 volts. Access times at 25°C for three different cases are displayed in Table 5.4 below.

Table 5.4 Access times for 3 different cases of input logic levels at 25°C.

VENDOR A

S/N	VCC (Volts)	TAVQV for CASE 1	TAVQV for CASE 2	TAVQV for CASE 3
	4.5	212 NS	212 NS	212 NS
11	5.0	212 NS	212 NS	212 NS
	5.5	213 NS	217 NS	213 NS
	4.5	232 NS	232 NS	231 NS
20	5.0	232 NS	232 NS	231 NS
	5.5	234 NS	234 NS	232 NS

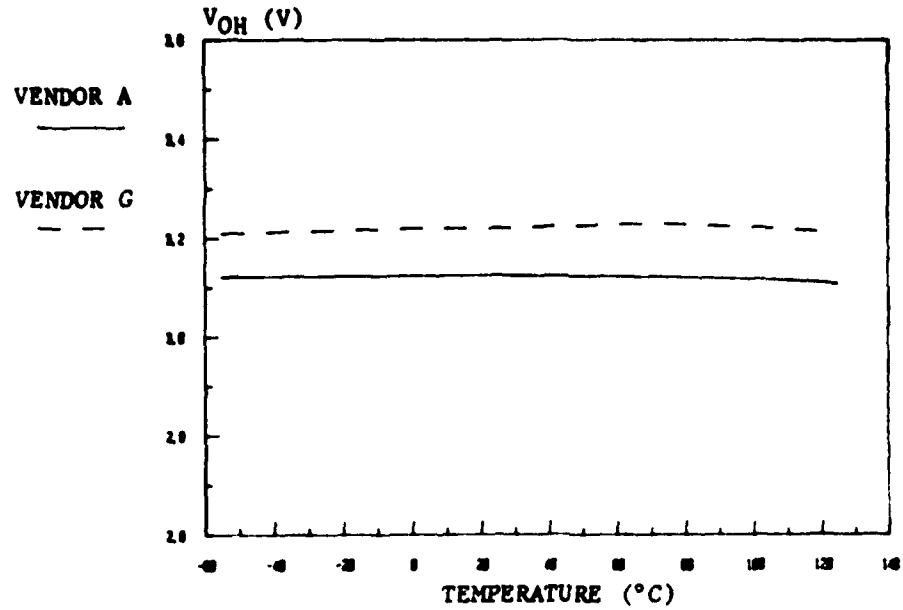


Figure 5.3a Average of Minimum V_{OH} Values

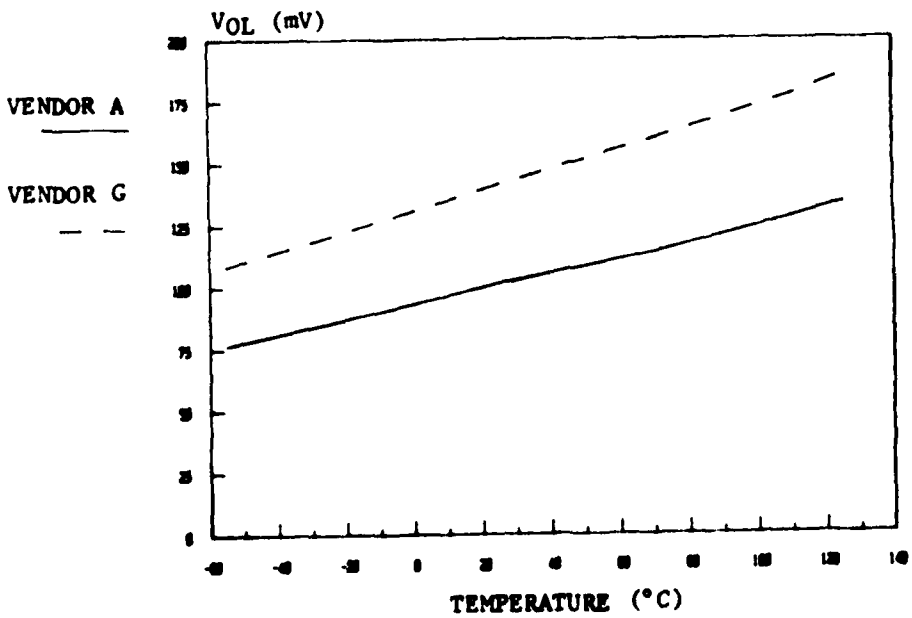


Figure 5.3b Average of Maximum V_{OL} Values

Table 5.4 Cont'

		VENDOR G		
S/N	VCC (Volts)	TAVQV for CASE 1	TAVQV for CASE 2	TAVQV for CASE 3
	4.5	141 NS	141 NS	141 NS
1	5.0	131 NS	131 NS	131 NS
	5.5	128 NS	128 NS	130 NS
	4.5	156 NS	155 NS	156 NS
5	5.0	141 NS	139 NS	141 NS
	5.5	127 NS	127 NS	128 NS

The data from Vendors A and G show little sensitivity to the three different logic level conditions.

Access time sensitivity due to varying supply voltage for the two vendors can also be seen in Table 5.4. For Vendor A, VCC had no significant impact on access time. Raising the supply voltage for Vendor G devices resulted in faster access times.

5.3.4 Supply Current (ICC)

Three supply current measurements were performed on each device at the six selected temperatures. They are as follows:

a.) ICC1 - measured while device is deselected (standby).
b.) ICC2 - measured while device is in active state.
c.) IPP1 - measured during READ.

All measurements of ICC1 and ICC2 for both vendors were well within their specified limits. Average values of ICC1 and ICC2 versus temperature, for both vendors, are plotted in Figure 5.4. The plots show that Vendor A devices have a slightly higher ICC1 than Vendor G devices, whereas Vendor G has a slightly higher ICC2 current than Vendor A.

The IPP1 measurement was taken while continuously performing READ operations. IPP1 was measured on all devices from each vendor. An IPP1 value per device and an average IPP1 per vendor is displayed in Table 5.5. This table gives a sample of 10 devices from each vendor. All measurements of IPP1 for both vendors were found to be well within the specified limit of 5mA.

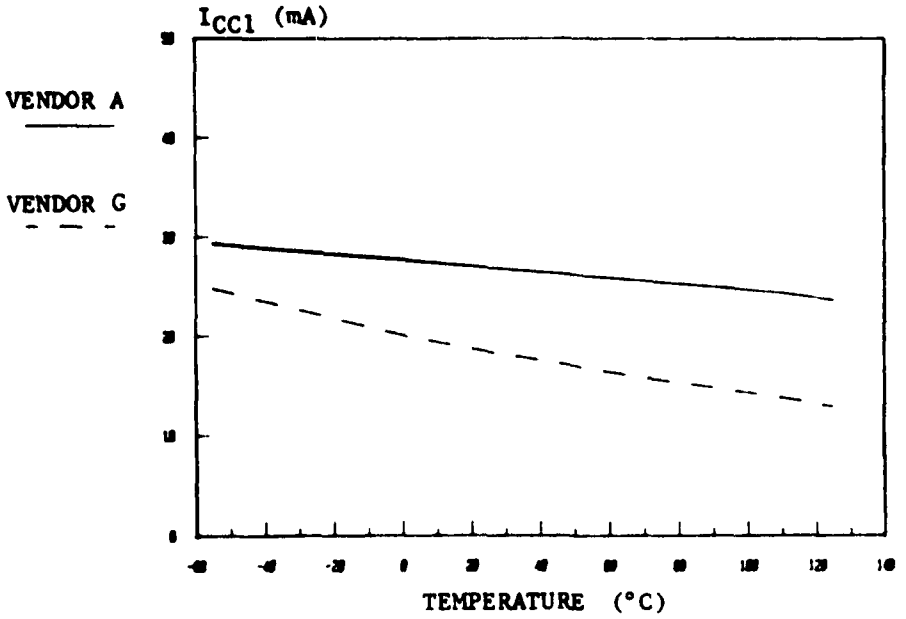


Figure 5.4a Average of I_{CC1}

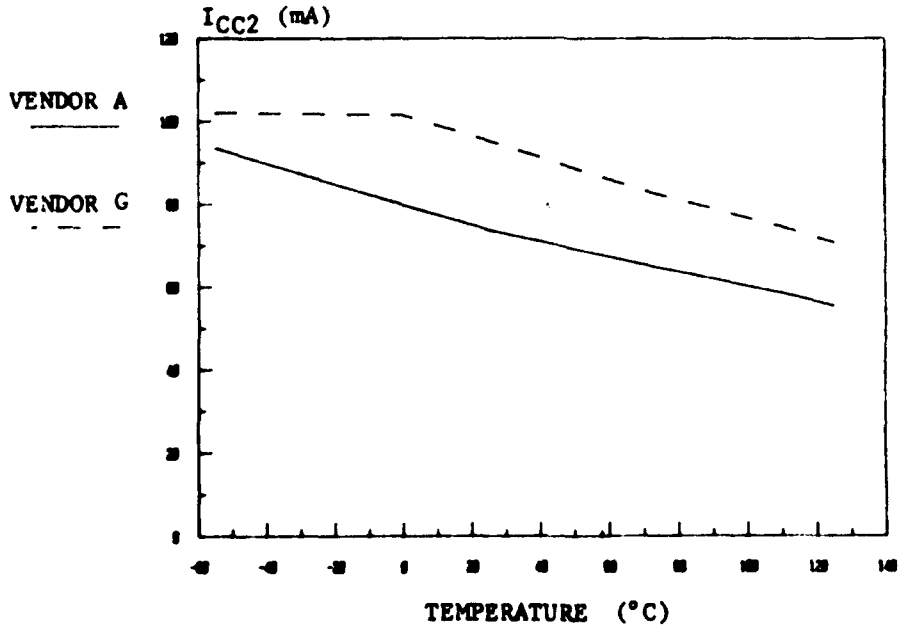


Figure 5.4b Average of I_{CC2}

Table 5.5 Average Values of IPP1 (Supply Current at Read)

Vendor A IPP1 (Supply Current at Read)			Vendor G IPP1 (Supply Current at Read)		
S/N	IPP1	Units	S/N	IPP1	Units
2	.808	mA	4	.742	mA
3	.758		5	.758	
4	.8		6	.775	
6	.808		7	.767	
7	.758		8	.7	
8	.85		9	.725	
9	.808		10	.775	
10	.808		11	.75	
11	.8		12	.767	
13	.8		13	.767	

IPP1 Vendor A Average = 0.8mA IPP1 Vendor G Average = 0.753mA

5.3.5 Input/Output Pin Capacitance

Capacitance measurements were performed on selected pins of three devices from each vendor. Table 5.6 lists the min,avg,max measurement data and the vendor specified limits. Both vendors' capacitance measurements fell below their maximum specified limits. Vendor A parts tend to have a lower capacitance per pin than Vendor G.

Table 5.6a Vendor A Min,Avg,Max Pin Capacitance

Pin	Min	Avg	Max	Limit	Unit
A0-A12	2.9	3.2	5	6	pf
O0-O7	4.2	5.3	6.5	12	pf
CE	3.2	3.2	3.2	6	pf
OE	3.0	3.0	3.0	6	pf

Table 5.6b Vendor G Min,Avg,Max Pin Capacitance

Pin	Min	Avg	Max	Limit	Unit
A0-A12	3.3	3.77	5.5	6	pf
O0-O7	6.8	8.0	9.2	12	pf
CE	3.4	3.4	3.4	6	pf
OE	3.2	3.2	3.2	6	pf

5.4 AC Characterization

Table 5.7 lists the AC parameters that were characterized and the vendor specified limits.

All AC measurements discussed in this section were made with output compare levels of 2.4V and 0.45V.

Table 5.7 Vendor Limits for AC Parameters

	Vendor A		Vendor G	
	Min	Max	Min	Max
TAVQV	-	450 nS	-	250 nS
TELQV	-	450 nS	-	250 nS
TOLQV	10 nS	150 nS	10 nS	100 nS
TAXQX	0 nS	-	0 nS	-

5.4.1 Vendor A AC Parameters

Four timing parameters were measured on Vendor A devices. They are TAVQV, TELQV, TOLQV, and TAXQX. These parameters were characterized under the following test conditions:

Temperature = -55, 0, 25, 70, 110, 125°C
VCC = 4.5V, 5.5V
VIL = 0.4V, VIH = 3.0V (CASE 1)
VIL = 0.6V, VIH = 2.4V (CASE 2)
VIL = 0.8V, VIH = 2.0V (CASE 3)

One parameter, TAXQX, exhibited no failures. When functional testing began, a significant number of TAVQV, TELQV, and TOLQV failures occurred at high VCC, low temperature and CASE 3 logic levels. Investigation showed that excessive amounts of ground noise (.4V to .6V peak) was present on the DUT ground. This problem was remedied by replacing the large zero insertion socket with single wire-wrap type socket pins. This brought the device extremely close to the ground plane of the test adapter and reduced the noise to a very low level, thus reducing the number of failures. However, as Table 5.8 indicates, Vendor A devices still exhibit sensitivity to low temperature and high VCC even after modification of the test adapter. Although input threshold measurements were not taken on these devices, it is suspected that Vendor A devices exhibit marginal logic high thresholds as do Vendor A EEPROMs. This condition prevents proper operation when small amounts of tester noise are present and Case 3 logic levels are used.

Table 5.8 Failures Remaining After Reducing Ground Noise

	# of Failures at Specified Temperature					
	-55°C	0°C	25°C	70°C	110°C	125°C
TAVQV at CASE 3, VCC=5.5V	9	1	0	0	0	0
TELQV at CASE 3, VCC=5.5V	17	2	1	0	0	0
TOLQV at CASE 3, VCC=5.5V	9	3	1	0	0	0

5.4.1.1 Address, Chip Enable, and Output Enable Access Times

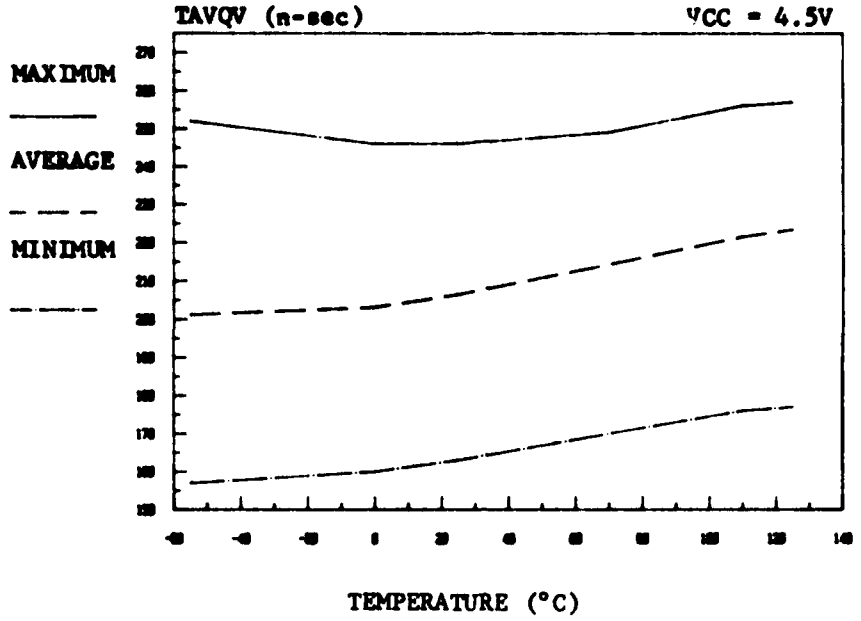
Minimum, Average, and Maximum plots of TAVQV are displayed in Figures 5.5 and 5.6 for two cases of logic levels. Plots of TAVQV for CASE 2 were not displayed because of the close similarity to CASE 1 results. TAVQV in Figure 5.5 increases slightly over the range of temperature. No significant difference in access time due to a change in VCC could be found. Figure 5.6 shows address access time for CASE 3 logic levels. At VCC = 4.5V the plot is very close to those at the other two cases of logic levels. However, at 5.5V TAVQV increases an average of 65 nsec from 0°C to -55°C. This sensitivity only becomes apparent at this worst case logic level.

Chip Enable Access Time (TELQV) is plotted in Figures 5.7, 5.8, and 5.9. Figure 5.7 displays TELQV for CASE 1 logic levels. At 4.5V, TELQV decreases from an average of 202 ns at 125°C to 144 ns at -55°C. For 5.5V the trend is the same except for the lower temperatures (0 to -55°C) where TELQV increases slightly. Figure 5.8 shows TELQV for CASE 2 logic levels. Here the trend is similar to that in CASE 1 except the sensitivity to low temperature at 5.5V is much more pronounced. For CASE 3 logic levels in Figure 5.9, the plot at 4.5V also displays this sensitivity. TELQV begins to increase from 155 ns at 70°C to 435 ns at -55°C. Since CASE 3 (VIH = 0.8V, VIL = 2.0V) is a worst case logic level, the sensitivity, if present, is expected to be at its greatest.

Figure 5.10 displays Output Enable Access Time (TOLQV) for CASE 2 logic levels. Plots of CASE 1 and CASE 3 are not displayed because of their similarity to CASE 2. As shown, the trend is for TOLQV to increase as temperature increases at both values of VCC.

5.4.1.2 Address to Invalid Output (TAXQX)

Plots of TAXQX for CASE 2 may be seen in Figure 5.11. As with TOLQV, plots of CASE 1 and CASE 3 logic levels are omitted due to their similarity to CASE 2. From the plot, TAXQX increases with an increase of temperature and does not change appreciably with a higher level of VCC.



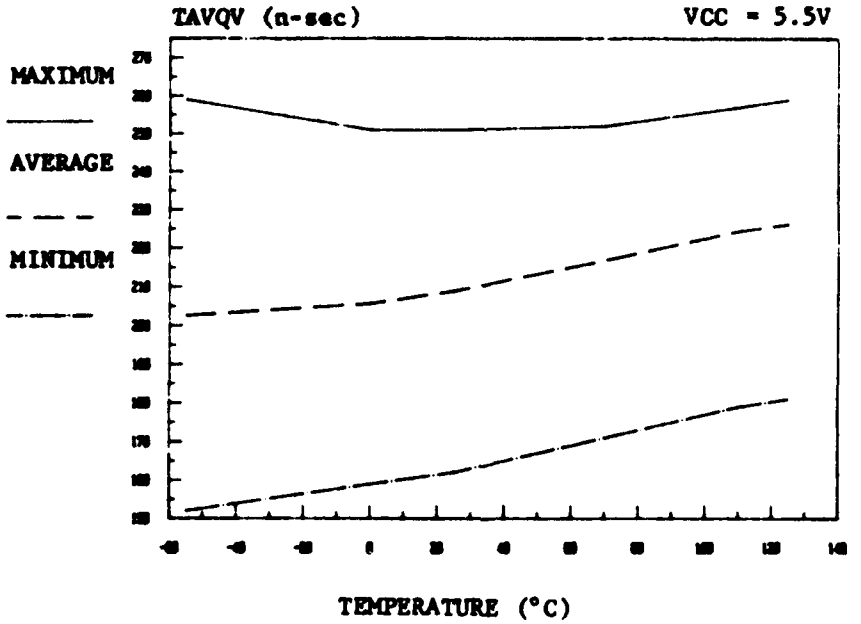
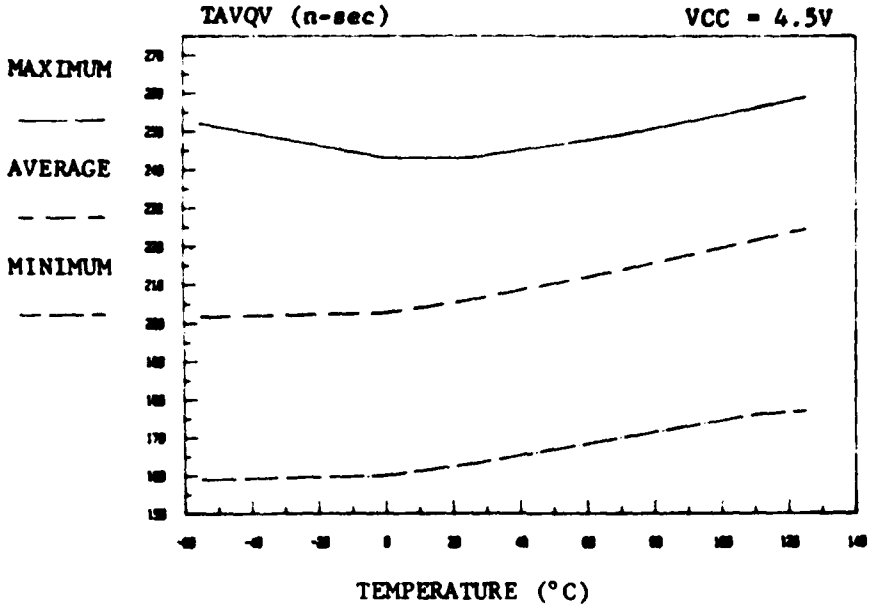


Figure 5.5 Vendor A - Address Access Time vs. Temperature for CASE 1 Logic Levels



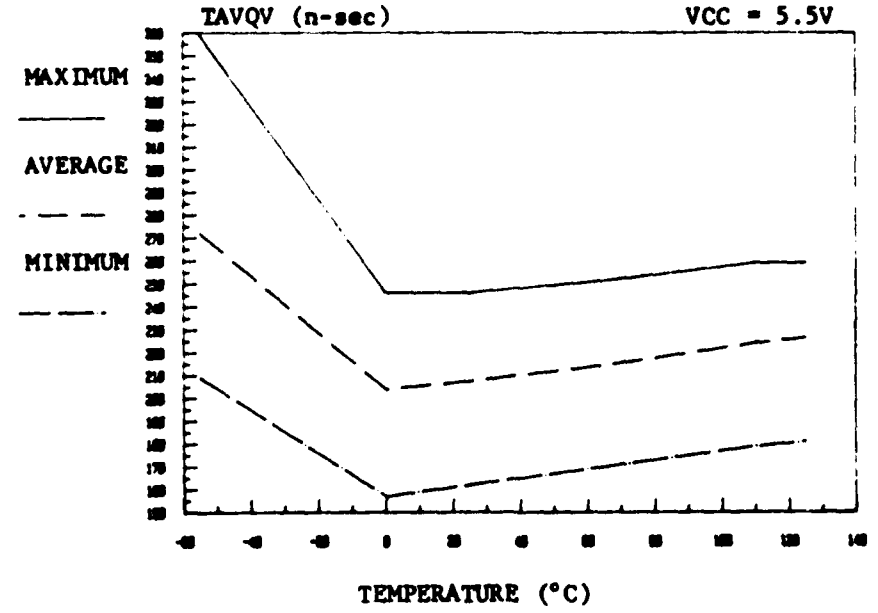
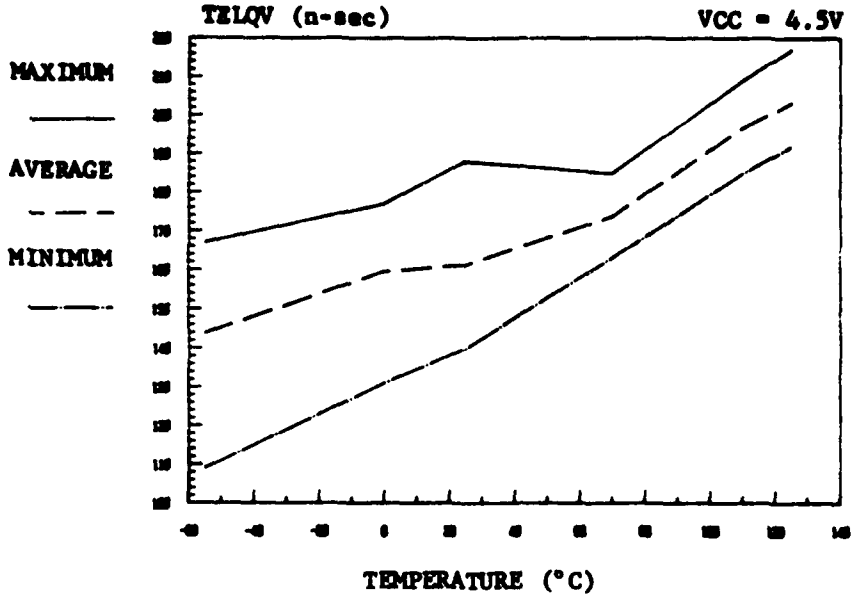


Figure 5.6 Vendor A - Address Access Time vs. Temperature for CASE 3 Logic Levels



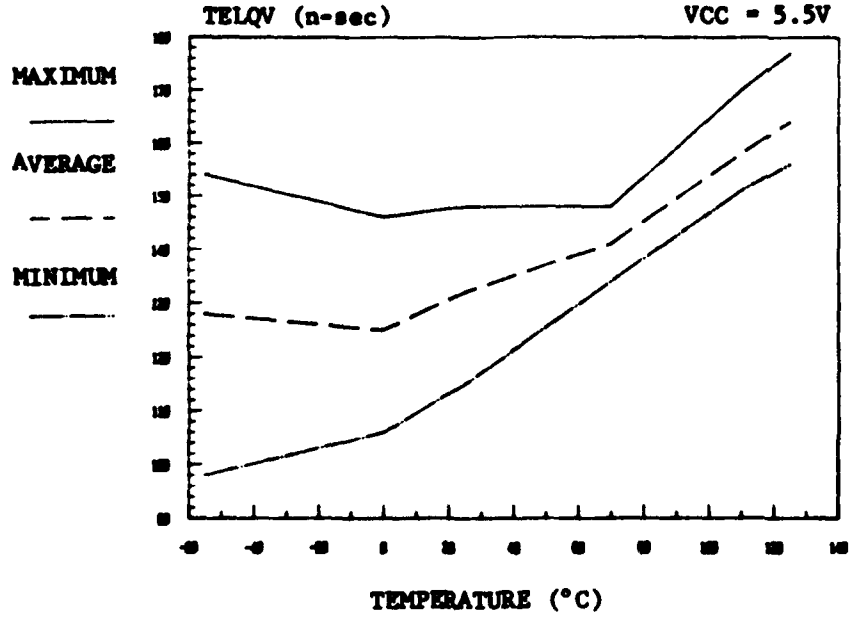
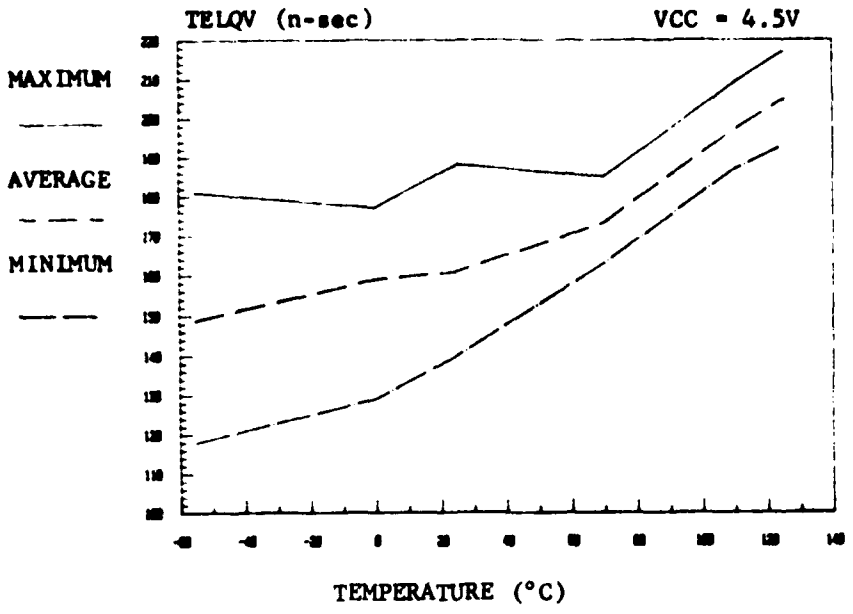


Figure 5.7 Vendor A - Chip Enable Access Time vs. Temperature for CASE 1 Logic Levels



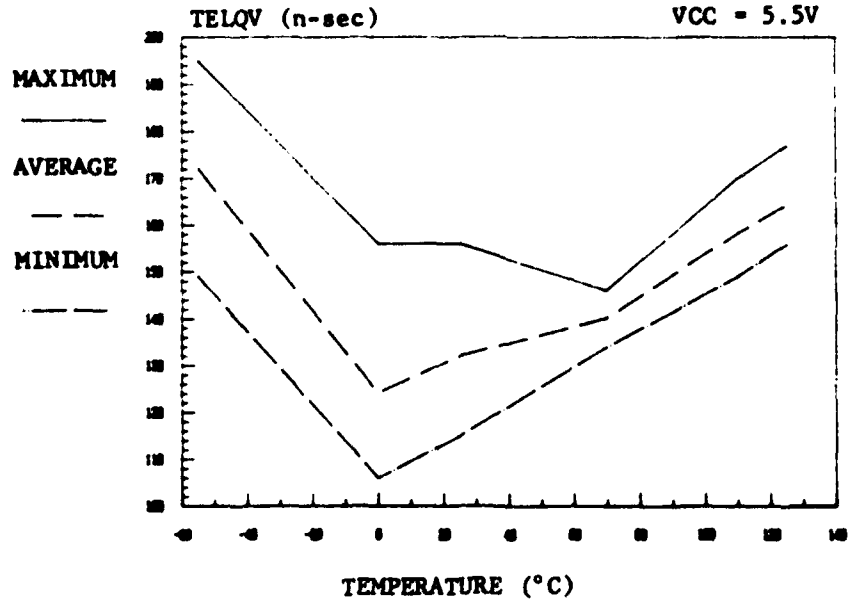
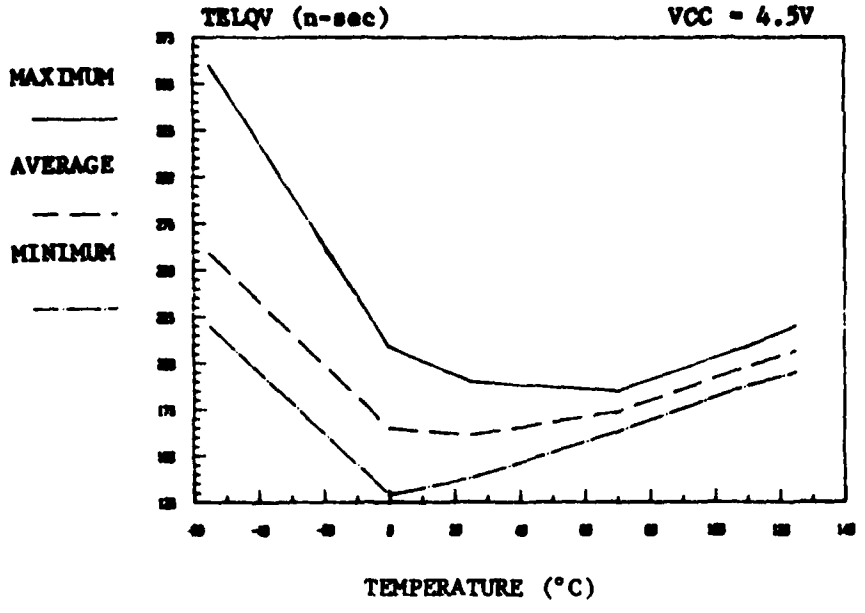


Figure 5.8 Vendor A - Chip Enable Access Time vs. Temperature for CASE 2 Logic Levels



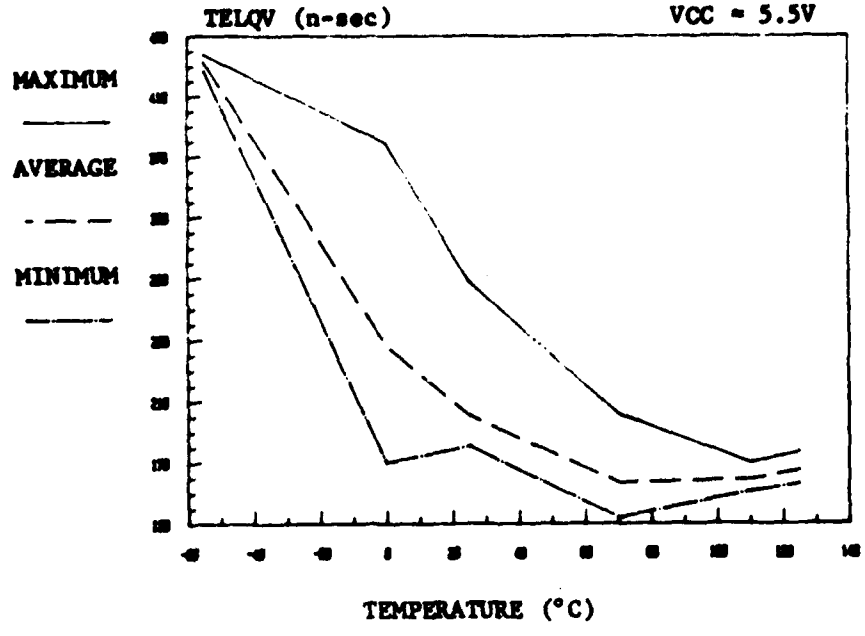
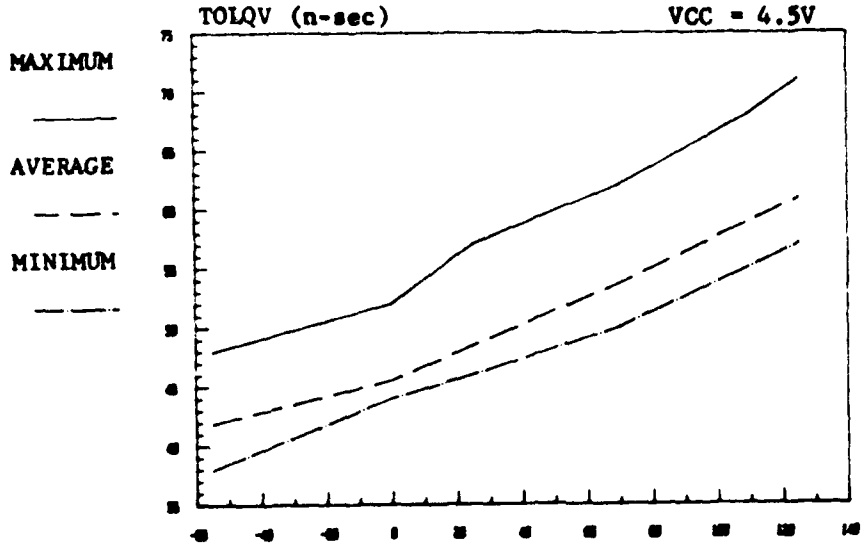


Figure 5.9 Vendor A - Chip Enable Access Time vs. Temperature for CASE 3 Logic Levels



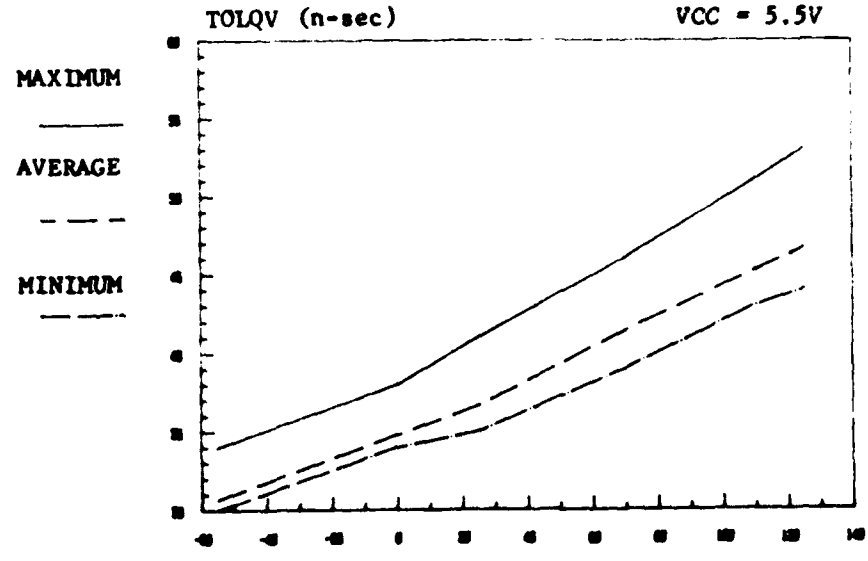


Figure 5.10 Vendor A - Output Enable Access Time vs. Temperature for CASE 2 Logic Levels

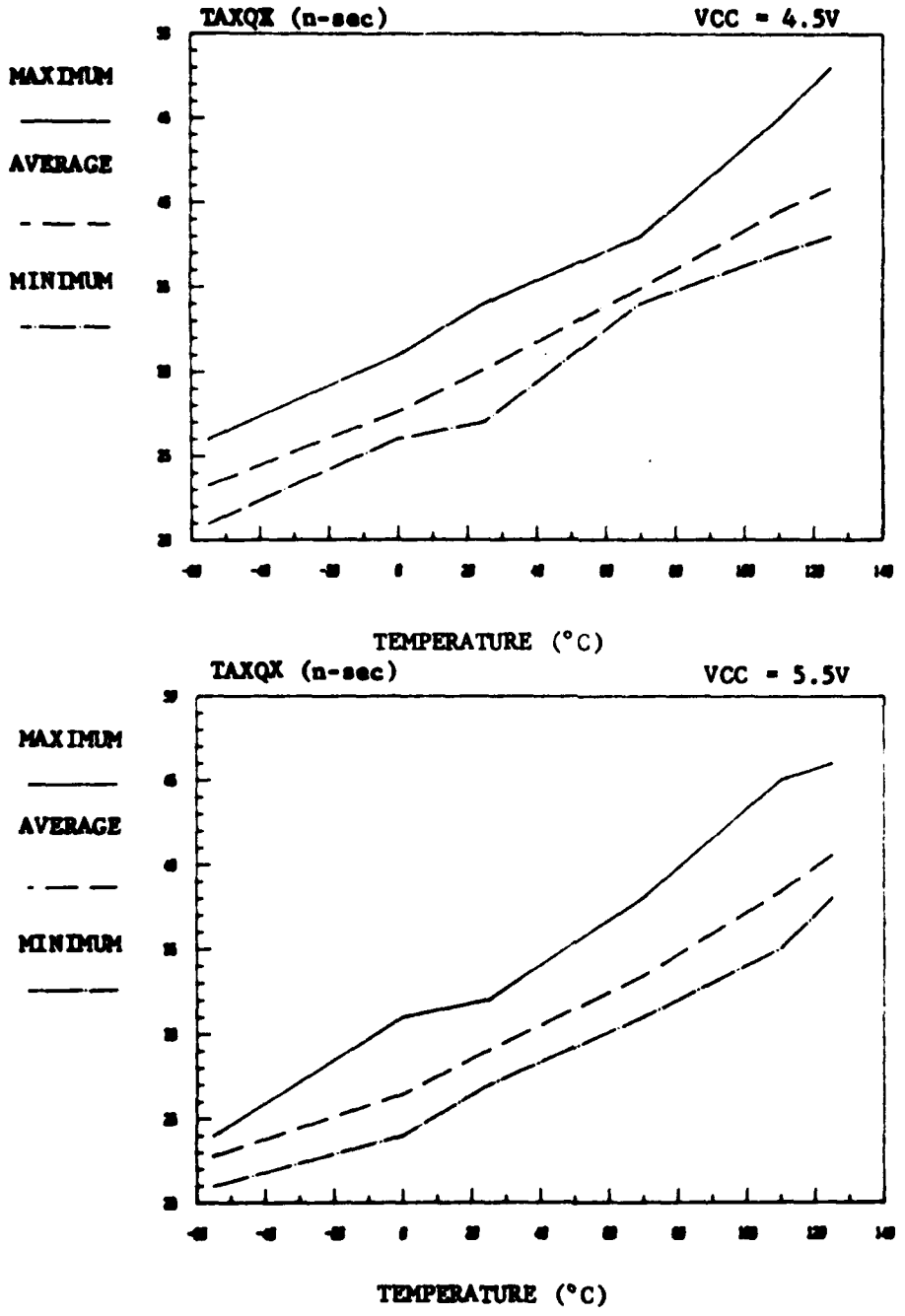


Figure 5.11 Vendor A - Address to Invalid Output vs. Temperature for CASE 2 Logic Levels

5.4.2 Vendor G AC Parameters

All Vendor G devices were well within their specified limits over the commercial temperature range (-25 to 85°C) and over the extended temperature range (-55 to 125°C). Vendor G parameters were characterized at CASE 3 logic levels. No parameter measurement exceeded the vendor specification for the four parameters; TAVQV, TELQV, TOLQV, and TAXQX.

5.4.2.1 Address, Chip Enable, and Output Enable Access Times

Figure 5.12 summarizes the measurement results of address access time (TAVQV) at VCC = 4.5V and VCC = 5.5V. Each set of three points at one temperature represents minimum (min), average (avg), and maximum (max) parameter values. The values at each temperature are for the 25 devices.

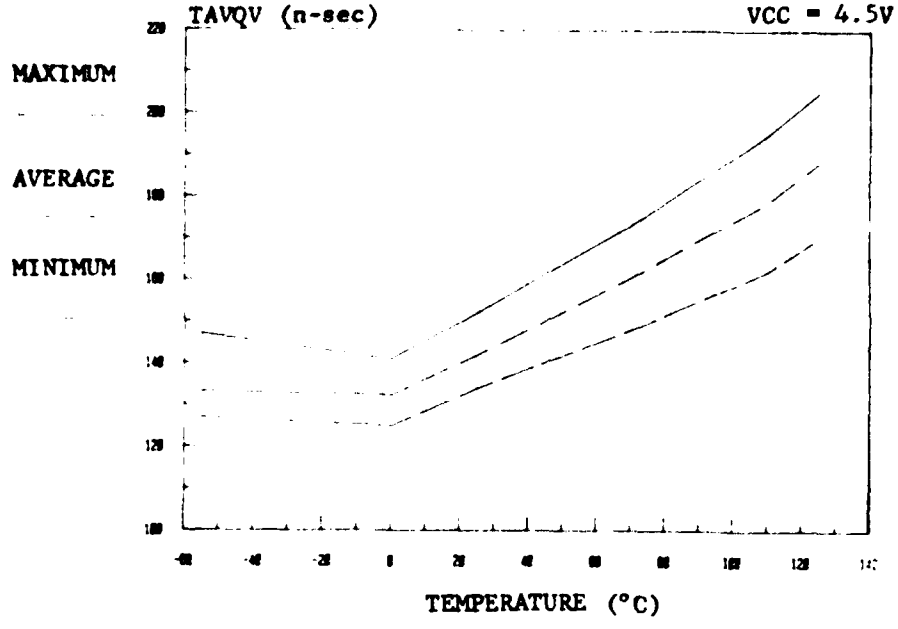
The plots of (TAVQV) for both cases of VCC display identical trends. Access time first decreases from -55 to 0°C then increases sharply from 0°C to 125°C. Access time at -55°C seems to be more sensitive at VCC = 5.5 volts than for VCC = 4.5 volts. At VCC = 5.5V, TAVQV is significantly lower than at VCC = 4.5V.

Figure 5.13 displays (min, max, avg) plots of chip enable access time (TELQV) at two cases of VCC. The sensitivity at -55°C seen for TAVQV is reversed here for TELQV. The plot of VCC = 4.5V displays a greater sensitivity to -55°C than the plots of VCC = 5.5V. The two plots of output enable access time (TOLQV) are shown in Figure 5.14. TOLQV is very similar for both cases of VCC. The major difference in the two cases is that TOLQV is lower by an average of 7.5 nsec for VCC = 5.5V than for VCC = 4.5V.

The plots of Address, Chip Enable, and Output Enable Access times illustrate that within the extended temperature range (-55 to 125°C) all devices meet their commercial specifications even though VCC is beyond the 4.75V minimum and 5.25V maximum vendor limits. A sensitivity for high VCC and low temperature was seen for TAVQV, while TELQV was sensitive at a low VCC and a low temperature.

5.4.2.2 Address to Invalid Output (TAXQX)

The plots in Figure 5.15 illustrate the minimum, average, and maximum values of the Address to Invalid Output parameter (TAXQX). The two curves displaying TAXQX at VCC = 4.5V and VCC = 5.5V are very similar. No appreciable difference can be seen over the entire temperature range of -55 to 125°C. At both VCC cases, TAXQX increases almost linearly from -55 to 125°C. Overall, TAXQX was well within the minimum commercial specification of 0 nsec.



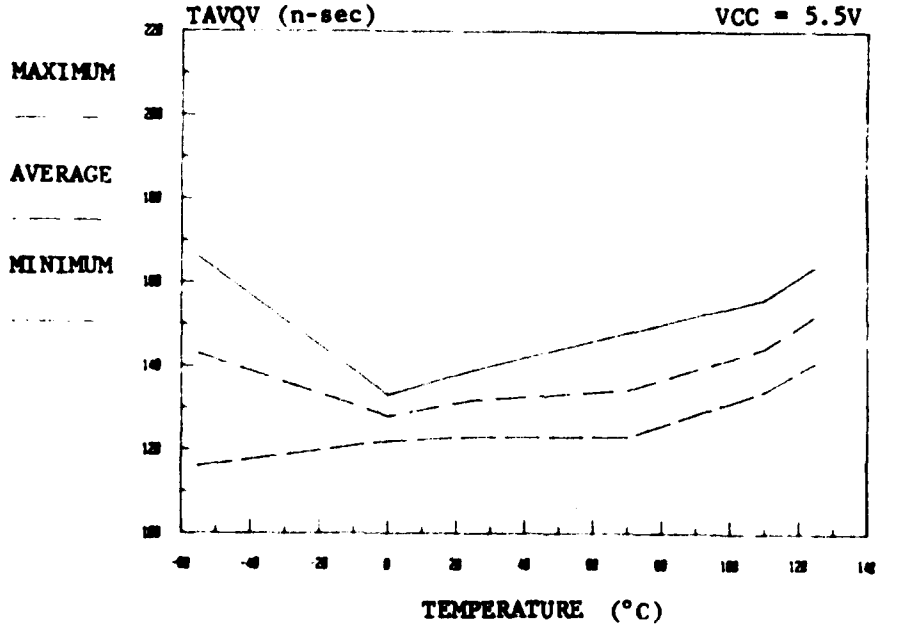
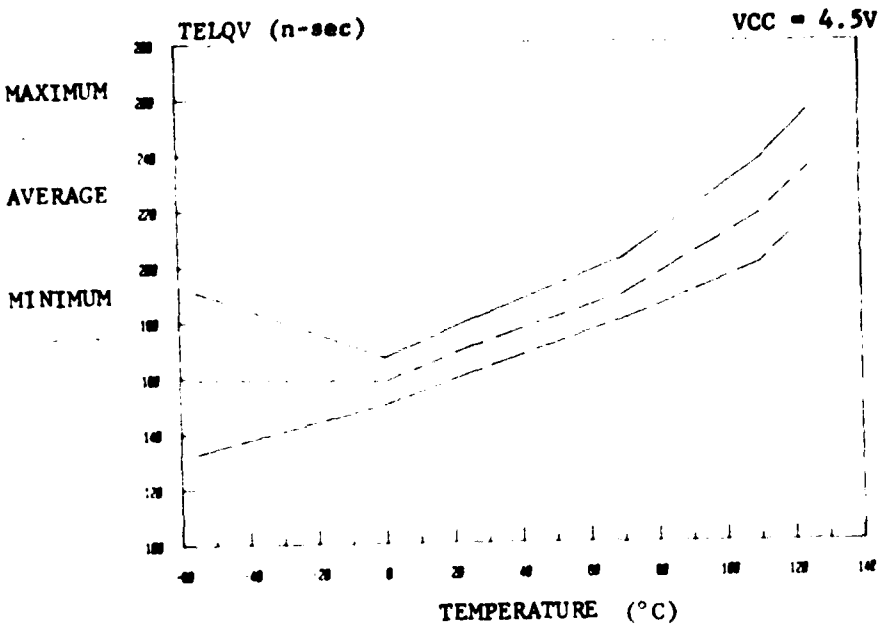


Figure 5.12 Vendor G - Address Access Time vs. Temperature



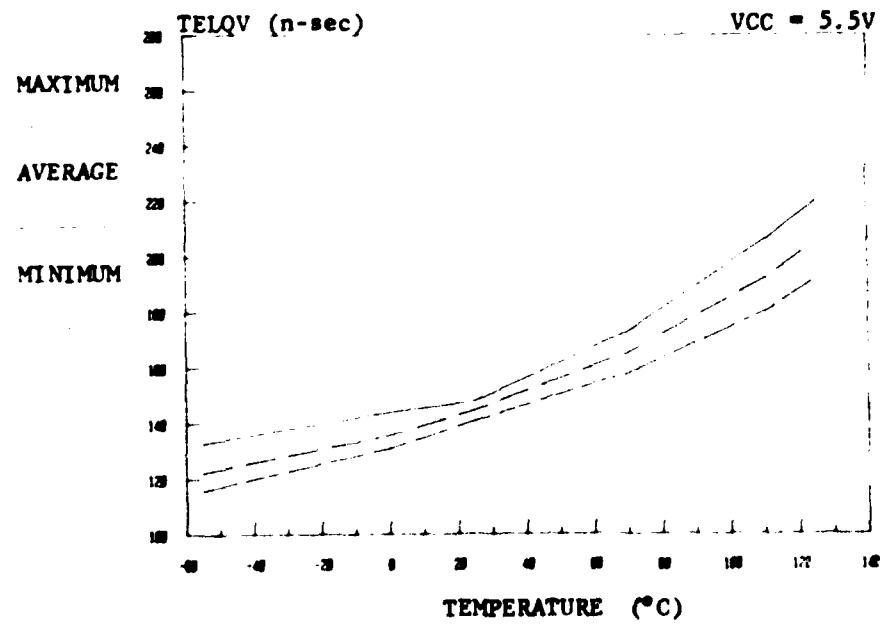
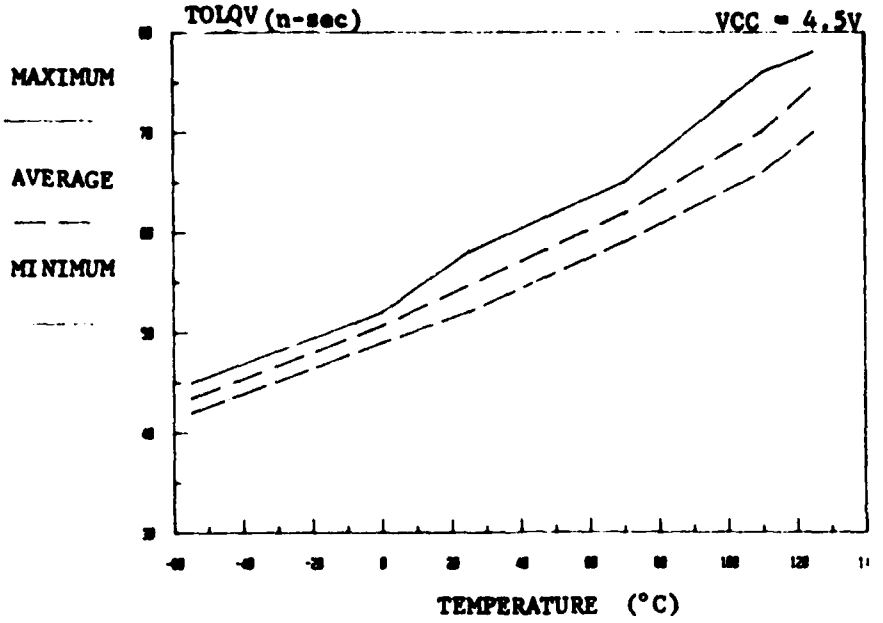


Figure 5.13 Vendor B - Chip Enable Access Time vs. Temperature



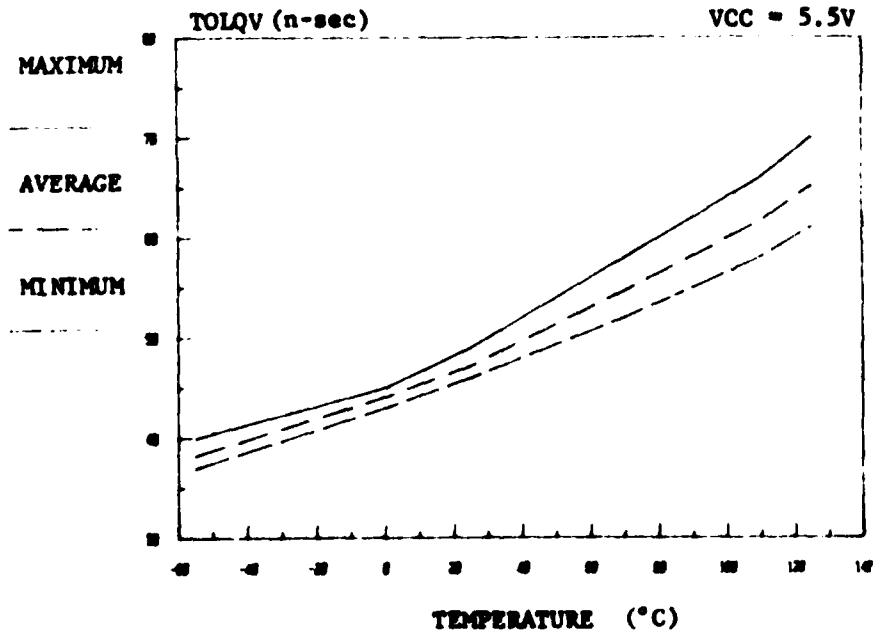
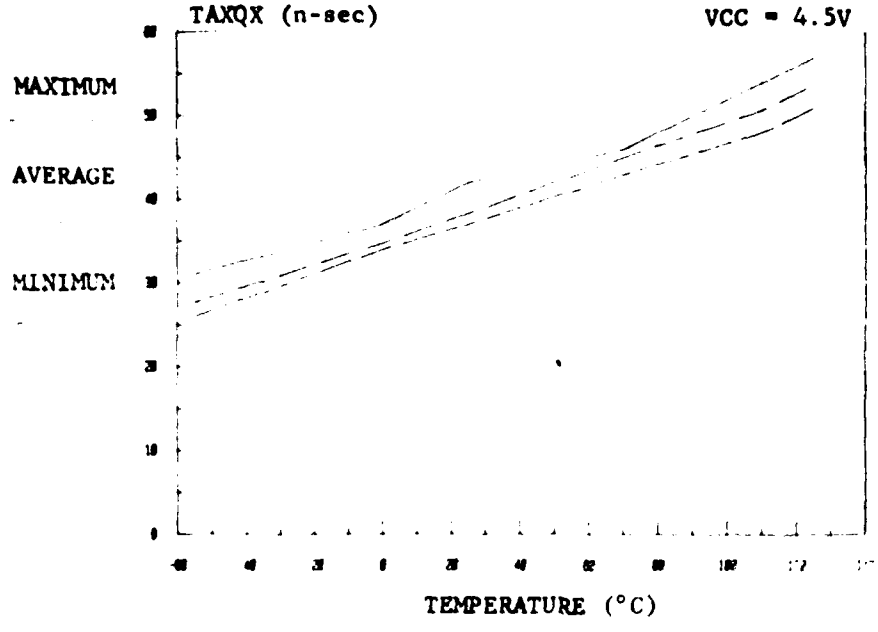


Figure 5.14 Vendor B - Output Enable Access Time vs. Temperature



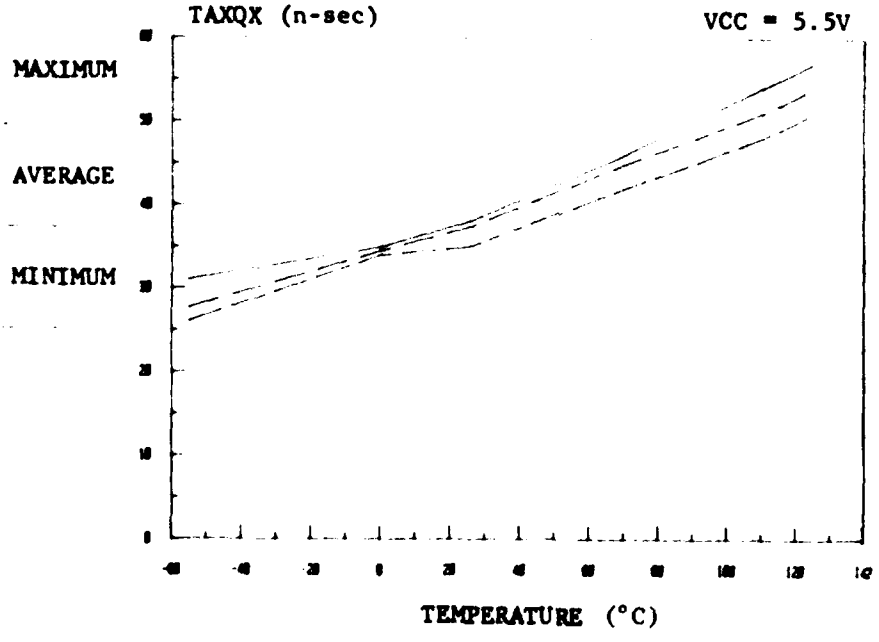


Figure 5.15 Vendor B - Address to Invalid Output Time vs. Temperature

5.4.3 Vendor A, Vendor G Output Disable Time (TOHQZ)

The current measurement method was used to determine the disable time of ten devices from each vendor.

Table 5.9a and 5.9b list data for Vendors A and G. A sample of ten devices from each vendor was tested in the VOH and VOL logic states. The only significant difference between vendors is that Vendor A is an average of 2 nsec faster than Vendor G. The output disable time is higher by an average of 5 nsec when the output is initially in the VOL logic state compared to an initial VOH state.

Table 5.9a Output Disable Time - Output initially at VOH

S/N	Vendor A TOHQZ		Vendor G TOHQZ	
1	15	nsec	16	nsec
2	16		16	
3	15		17	
4	14		18	
8	15		17	
9	14		18	
10	14		17	
13	14		17	
14	14		16	
20	15		17	

Table 5.9b Output Disable Time - Output initially at VOL

S/N	Vendor A TOHQZ		Vendor G TOHQZ	
1	22	nsec	21	nsec
2	23		22	
3	23		22	
4	20		24	
8	22		23	
9	21		24	
10	20		24	
13	20		23	
14	20		24	
20	22		23	

5.4.4 AC Characterization Summary

In general, Vendor A devices are slower than Vendor G except for output disable time(TOHQZ). At 5.5V, TAVQV, TELQV, and TOLQV times tended to increase. No appreciable change was noted in TAXQX at VCC=5.0 volts.

5.5 Pattern Sensitivity

March, Address Complement, Row-Column Complement, and Gallop test patterns were implemented on six devices from each vendor to determine their address access time sensitivity at 25°C. Data was accumulated at VCC = 4.5V and VCC = 5.5V. The following cases of logic levels were used in this test:

CASE 1: VIH = 3.0V, VIL = 0.4V
CASE 2: VIH = 2.0V, VIL = 0.8V

Table 5.10 displays worst case access times for the four test patterns at each set of logic levels. Each value in the table represents the average access time for the six devices from each vendor. The access time from pattern to pattern does not differ appreciably for either vendor. For example, Vendor A at CASE 1 and VCC = 4.5V, the access time for the March pattern is 203 ns, whereas the Gallop pattern yielded 207ns. This difference is insignificant when considering the execution times of the two patterns. The Gallop pattern is frequently considered worst case because of the address decoder activity it generates. However, the execution time is approximately 9 minutes as compared to 3-5 sec for the March. To isolate an access time limit using Gallop required eight successive test executions for a total elapsed time of over one hour. The March and Address patterns take seconds to execute. The Row-Column complement test pattern execution time was also a matter of seconds.

The Address complement and Row-Column Complement patterns, unlike the March pattern, provide complementing action each memory cycle. Because the Row-Column Complement pattern, along with the data pattern in Figure 2.2, verifies address uniqueness, it is recommended for the slash sheet.

Table 5.10a Vendor A Pattern Sensitivity

Vendor A	TAVQV, CASE 1 VCC = 4.5V	TAVQV, CASE 1 VCC = 5.5V	TAVQV, CASE 2 VCC = 4.5V	TAVQV, CASE 2 VCC = 5.5V
March	203 ns	206 ns	203 ns	206 ns
Address Complement	206 ns	209 ns	206 ns	209 ns
Row-Column Complement	204 ns	207 ns	205 ns	208 ns
Gallop	207 ns	209 ns	205 ns	208 ns

Table 5.10b Vendor G Pattern Sensitivity

Vendor G	TAVQV, CASE 1 VCC = 4.5V	TAVQV, CASE 1 VCC = 5.5V	TAVQV, CASE 2 VCC = 4.5V	TAVQV, CASE 2 VCC = 5.5V
March	149 ns	132 ns	150 ns	129 ns
Address Complement	150 ns	131 ns	150 ns	132 ns
Row-Column Complement	148 ns	129 ns	149 ns	130 ns
Gallop	149 ns	132 ns	149 ns	132 ns

5.6 Programming Parameters

Programming parameters were tested at 25°C for VCCs of 4.5V, 5.0V, and 5.5V and VPP programming voltages of 15V, 17V, 21V, and 22V. Two devices from each vendor were tested at each level of VCC. This test consisted of fixing the parameter to be tested at a value that would verify the manufacturer's limits. This was performed while keeping the other programming parameters at a nominal value. Sixty-four (64) byte locations were then programmed at each VPP. This resulted in a total of 256 programmed locations for each fixed programming parameter value at each VCC per device. The programming integrity of the parameter tested was then verified by checking the state of the programmed byte locations.

The programming parameters and the values they were verified at are as follows:

1. Address Setup Time (TAVPL) 0us, 1us, 2us
2. Chip Enable Setup Time (TELPL) 0us, 1us, 2us
3. Data Setup Time (TDVPL) 0us, 1us, 2us
4. Data Hold Time (TPLDZ) 0us, 1us, 2us
5. VPP Setup Time (TVVPL) 0us, 1us, 2us
6. PGM Pulse Width (TPLPH) 0us, 1us, 2us

Table 5.11 lists each vendor's programming parameters and the specified limits. All programming verifications were made with output compare levels of 2.4V and 0.4V.

Table 5.11 Manufacturer's Specified Limits for Programming Parameters

Parameter	Vendor A		Vendor G		Units
	Min	Max	Min	Max	
TAVPL	2	-	2	-	usec
TELPL	2	-	2	-	
TDVPL	2	-	2	-	
TPLDZ	2	-	2	-	
TVVPL	2	-	2	-	
TPLPH	45	55	45	55	usec
VPP	20.5	21.5	20.5	21.5	V

Table 5.12 below shows the results of the characterization. The table displays the number of programmed bytes out of a possible sixty-four (64) for each test condition. Each value represents an average of two devices per VCC.

From the table, Vendor A devices display little programmability at VPP = 17V and VCC = 4.5V. As VCC increases from 4.5V to 5.5V, a notable increase in programmed cells occur. At a VCC of 5V, the number of cells programmed at VPP = 17V is an average of 26% of the maximum. For VPPs of 21V and 22V, 100% of the cells were found to be programmed over the entire range of VCC. No significant change in programmability could be seen when program parameter timing was varied.

Vendor G devices also show some degradation of programming integrity at VPP = 17V. At this VPP and a VCC of 4.5V, 99% of the cells programmed. As VCC increased, the number of unprogrammed cells at VPP = 17V decreased. All cells were found to be programmed at VPPs of 21V and 22V over the range of VCC. No significant change in programmability could be seen over each parameter's range of fixed values.

For both vendors, programming integrity was also checked at a VPP of 15 volts. No cells in any device from either vendor programmed at this voltage.

Table 5.12a Vendor A - Number of Programmed Bytes for Various Programming Conditions

Parameter (at fixed value)	VCC=4.5V VPP=17	21	22	VCC=5.0V VPP=17	21	22	VCC=5.5V VPP=17	21	22
TAVPL (2us)	1	*	*	25	*	*	30	*	*
TAVPL (1us)	0	*	*	22	*	*	30	*	*
TAVPL (0us)	0	*	*	19	*	*	30	*	*
TELPL (2us)	0	*	*	19	*	*	30	*	*
TELPL (1us)	0	*	*	22	*	*	25	*	*
TELPL (0us)	0	*	*	15	*	*	27	*	*
TDVPL (2us)	0	*	*	18	*	*	24	*	*
TDVPL (1us)	0	*	*	15	*	*	28	*	*
TDVPL (0us)	0	*	*	17	*	*	28	*	*
TPLDZ (2us)	0	*	*	12	*	*	27	*	*
TPLDZ (1us)	0	*	*	18	*	*	27	*	*
TPLDZ (0us)	0	*	*	13	*	*	25	*	*
TVVPL (2us)	0	*	*	14	*	*	21	*	*
TVVPL (1us)	4	*	*	31	*	*	44	*	*
TVVPL (0us)	0	*	*	14	*	*	24	*	*
TPLPH (40ms)	0	*	*	3	*	*	6	*	*
TPLPH (45ms)	0	*	*	12	*	*	19	*	*
TPLPH (55ms)	0	*	*	4	*	*	30	*	*

Note: * represents all 64 byte locations programmed.

Table 5.12b Vendor G - Number of Programmed Bytes for Various Programming Conditions

Parameter (at fixed value)	VCC=4.5V VPP=17	21	22	VCC=5.0V VPP=17	21	22	VCC=5.5V VPP=17	21	22
TAVPL (2us)	62	*	*	*	*	*	*	*	*
TAVPL (1us)	63	*	*	*	*	*	*	*	*
TAVPL (0us)	63	*	*	*	*	*	*	*	*
TELPL (2us)	64	*	*	*	*	*	*	*	*
TELPL (1us)	*	*	*	*	*	*	*	*	*
TELPL (0us)	*	*	*	*	*	*	*	*	*
TDVPL (2us)	*	*	*	*	*	*	*	*	*
TDVPL (1us)	*	*	*	*	*	*	*	*	*
TDVPL (0us)	*	*	*	*	*	*	64	*	*
TPLDZ (2us)	*	*	*	*	*	*	63	*	*
TPLDZ (1us)	*	*	*	*	*	*	*	*	*
TPLDZ (0us)	*	*	*	*	*	*	*	*	*
TVVPL (2us)	*	*	*	*	*	*	*	*	*
TVVPL (1us)	*	*	*	*	*	*	*	*	*
TVVPL (0us)	*	*	*	*	*	*	*	*	*
TPLPH (40ms)	58	*	*	64	*	*	62	*	*
TPLPH (45ms)	63	*	*	*	*	*	63	*	*
TPLPH (55ms)	63	*	*	*	*	*	*	*	*

Note: * represents all 64 byte locations programmed.

5.7 Erasure Characteristics

Six devices from each vendor were subjected to ultraviolet light (253.7nm at 6700uW/cm^2) for increasing intervals of time to determine their erasure characteristics. Each device had been programmed using the values of parameters given in the programming parameter characterization described in section 5.6.

Table 5.13 summarizes the erasure time data. Erasure times shown are correlated to the six programming parameters that were each applied to certain cell locations in the device.

It is concluded, as one may suspect, that erasure time is indicative of the relative amount of charge stored during programming. The amount of charge stored is affected most by the VPP amplitude and not significantly affected by pulse width or setup and hold times.

Table 5.13 Erasure Time (in seconds) of Six Devices for Various Programming Parameters and Voltages

	Vendor A			Vendor G		
	VPP			VPP		
	17V	21V	22V	17V	21V	22V
TAVPL (2usec)	5	90	90	40	90	90
TAVPL (1usec)	5	90	120	40	90	90
TAVPL (0usec)	5	90	120	40	90	90
TELPL (2usec)	5	90	120	40	90	90
TELPL (1usec)	5	120	120	40	90	90
TELPL (0usec)	5	90	120	40	90	90
TDVPL (2usec)	5	120	120	40	90	90
TDVPL (1usec)	5	120	120	40	90	90
TDVPL (0usec)	5	120	120	40	90	90
TPLDZ (2usec)	5	90	120	40	90	90
TPLDZ (1usec)	5	90	120	40	90	90
TPLDZ (0usec)	5	90	120	40	90	90
TVVPL (2usec)	5	90	120	40	90	90
TVVPL (1usec)	5	90	120	40	90	90
TVVPL (0usec)	5	90	120	40	90	90
TPLPH (40ms)	5	90	120	40	90	90
TPLPH (45ms)	5	90	120	40	90	90
TPLPH (44ms)	5	120	120	40	90	90

5.8 Bake

High temperature bake of UV-EPROMS helps to accelerate the loss of stored charge in a programmed cell. Data retention of the device at high temperature can be determined in this way.

A static bake was performed on six devices from each vendor. The bake test consisted of programming the devices with a data pattern prior to high temperature bake. Once programmed, the devices were placed in an oven at 150°C. After 48 hours the devices were removed from the oven and the programmed pattern was verified at 25°C.

This bake cycle was repeated six times for both vendors giving a total bake time of 288 hours. During this period of time there was no loss of data from any of the devices.

6. 16K Registered Output PROM

6.1 Introduction

The 27S45 is a Registered Output PROM employing fusible links of Platinum-Silicide (PtSi). The memory array is configured 2K x 8 and has an 8 bit register with tri-state outputs. The output enable line (E/E's) may be programmed to be synchronous or asynchronous depending on the particular application requirements. A programmable initialize word (2049th memory location) may be loaded onto the output asynchronously by pulling the initialize input low. A photograph of the die from Vendor H is shown in Figure 6.1. Table 6.1 lists device part number, quantities, and date code. Table 6.2 lists the die size. A block diagram of the 27S45 is shown in figure 6.3.

Sources for the device included AMD (27S45) and Texas Instruments (28R166). Although 28R166's were ordered from Texas Instruments, availability problems precluded the characterization of this device. AMD (Vendor H) responded by sending fifteen 27S45's whose characterization is the focus of this section.

Table 6.1 Devices Provided for Characterization

Vendor	Part No.	Date Code	Quantity
H	27S45	8244	15

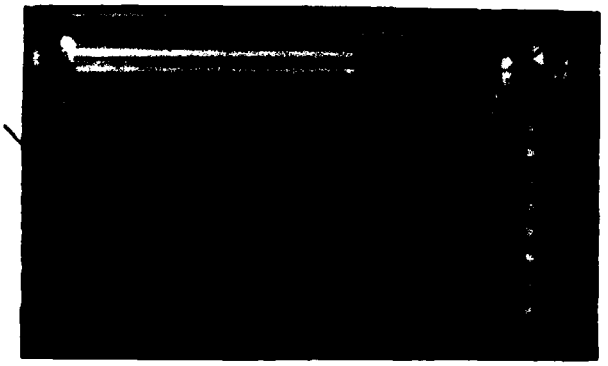
Table 6.2 16K Registered Output PROM Chip Dimensions

Vendor	Length (mm)	Width (mm)	Area (sq. mm)
H	5.61	3.43	19.24

6.2 Incoming Test

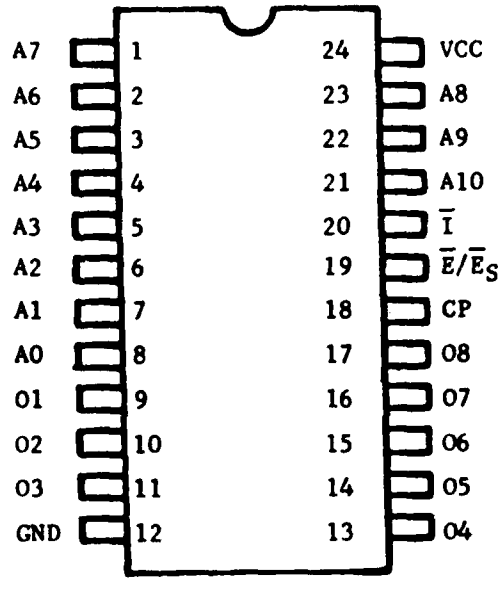
Unprogrammed device cells store a logic low. Upon receipt, all devices were blank checked to verify that no fuses had been programmed. No failures occurred during this incoming test procedure.

Programming of the Registered Output PROMs was accomplished on the S-3270. Since the access time of a registered output PROM is actually the delay from the register clock to its output, pattern sensitivity is essentially non-relevant. In view of this fact, use of the PROM pattern specified in the 'data patterns' section of this report was not required. For the sake of simplicity all devices were programmed with an alternating checkerboard pattern.



VENDOR H

FIGURE 6.1 DIE PHOTO - 2K X8 FPROM (14.84X)



Vendor H

Figure 6.2 16K Registered Output PROM Pin Configuration

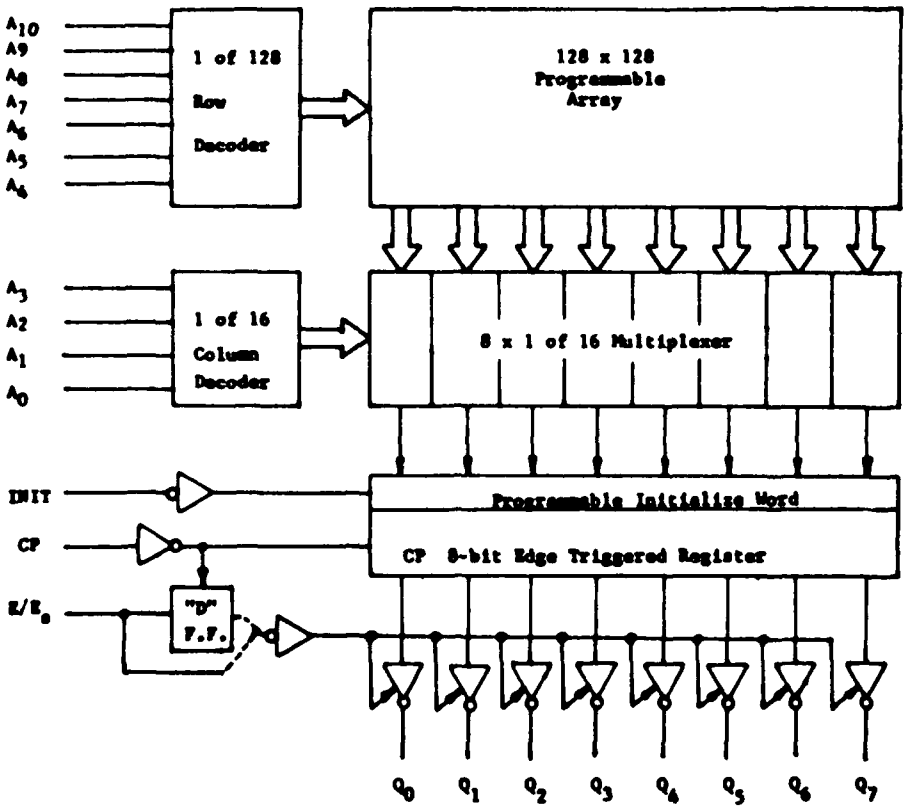


Figure 6.3 27S45 Block Diagram

6.3 DC Parameters

Table 6.3 lists the vendor specified DC Parameters and their respective limits.

Table 6.3 Vendor Specified DC Parameters

Symbol	Parameter	Min	Max	Units
VCC	Supply Voltage	4.75	5.25	V
ICC	Supply Current		185	mA
IIL	Input Leakage Current Low		-250 VIN=0.45V	uA
IIH	Input Leakage Current High		40 VIN=VCC	uA
ICEX	Output Leakage (Tri-State)		+/-40	uA
VIC	Input Clamp Diode Voltage		-1.2 IIN=-18mA	V
VOL	Low Level Output Voltage		0.5 IOL=16mA	V
VOH	High Level Output Voltage	2.4 IOH=-2mA		V
IOS	Output Short Circuit Current	-20	-90	mA

6.3.1 Leakage Current (IIL, IIH)

IIH measurements were significantly less than the 40uA maximum vendor specified limit over the full military temperature range(See Figure 6.4). IIL measurements were slightly less than the vendor specified typical of -20uA but much less than the maximum specification of -250uA. Average values ranged from -12.5uA at -55°C and increased to -9.5uA at +125°C.

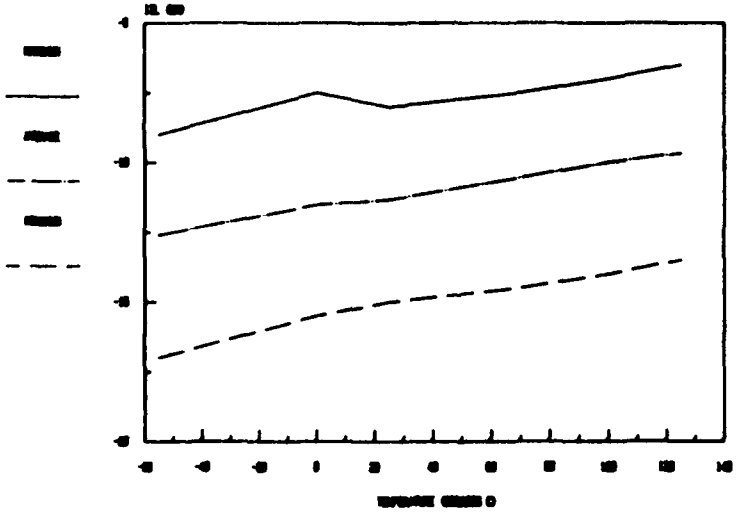


Figure 6.4 Input Leakage Current Low Level (IIL)

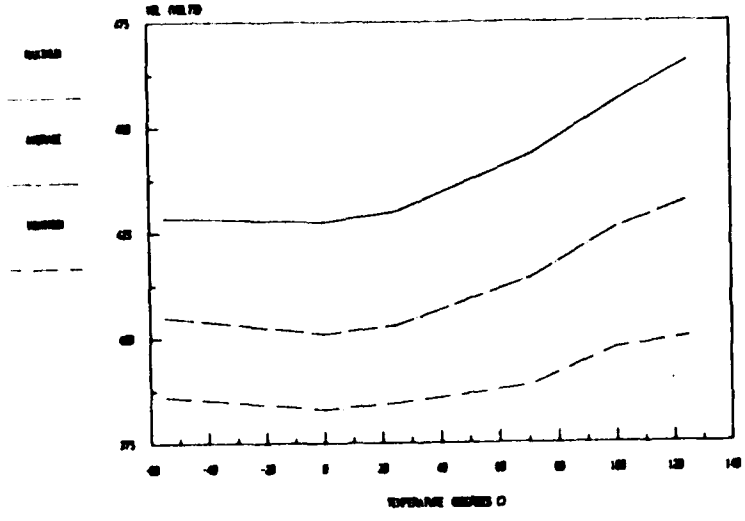


Figure 6.5a Output Voltage Low Level

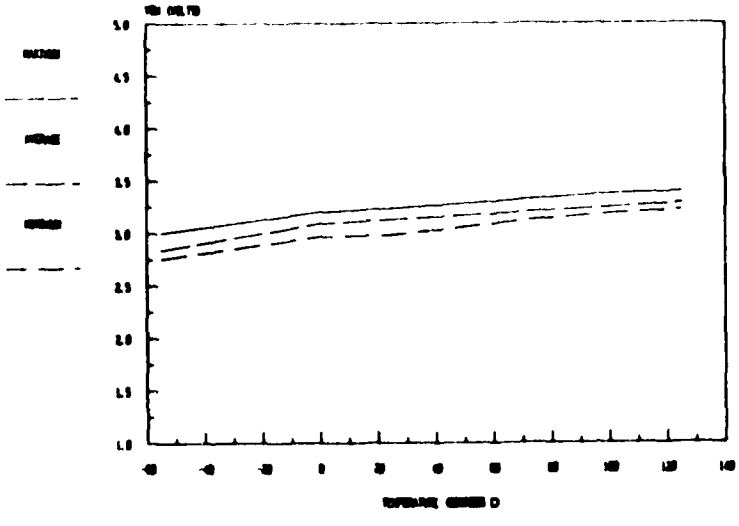


Figure 6.5b Output Voltage High Level

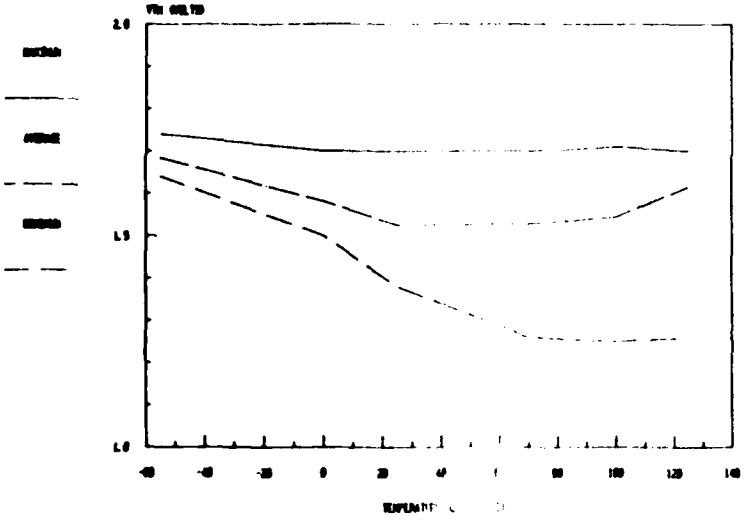


Figure 6.6 Input Voltage Threshold

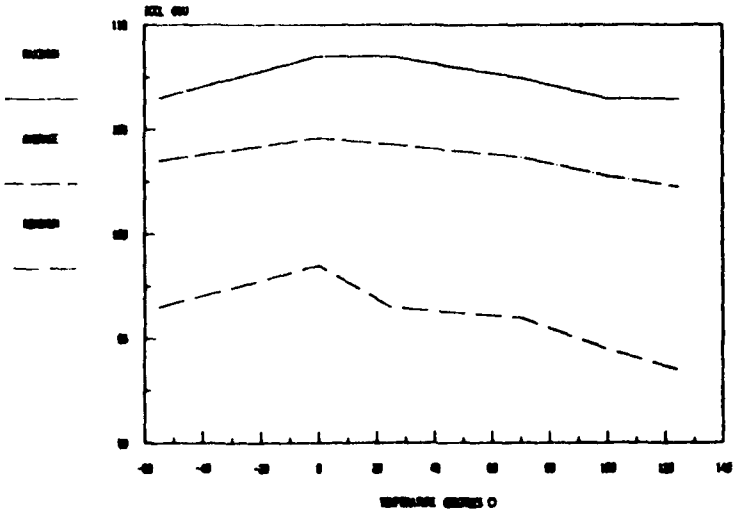


Figure 6.7a Supply Current at VCC = 4.5V (ICCL)

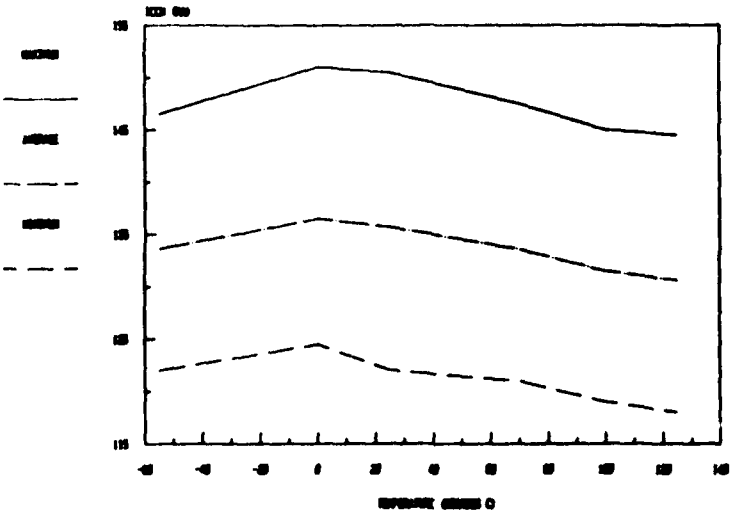


Figure 6.7b Supply Current at VCC = 5.5V (ICCH)

6.3.2 Logic Output Voltage (VOL, VOH)

The output voltage low (VOL) specification for the 27845 is 0.5V maximum. The average VOL measurement was 400mV at -55°C which increased to 430mV at +125°C. Again, this was sufficiently below the specified maximum (See Figure 6.5). The VOH parameter's sensitivity to temperature was significantly more pronounced. The average VOH measurement of 2.84V at -55°C increased to 3.28V at +125°C in a non-linear fashion. Although this parameter displays a fair amount of sensitivity to temperature, it sufficiently exceeds the manufacturers specified minimum of 2.4V and therefore presents no problem.

6.3.3 Input Threshold Voltage (VIL,VIH)

The variation of the average input threshold voltage over the full temperature range was 150mV. The curves shown in Figure 6.6, indicate a spread of less than 125mV at -55°C which increases to 450mV at +125°C. This wide variation at +125°C is due to a few parts that exhibit more temperature sensitivity than the rest. Despite this variation among devices, the input voltage threshold is still well within the VIL to VIH band (0.8 max to 2.0V min) specified by the vendor.

6.3.4 Supply Current (ICCL, ICCH)

Supply current, at 4.5V and 5.5V respectively, generally decreased with increasing temperature(Figure 6.7). The average values for ICCL and ICCH over the full temperature range were 104mA and 185mA max. The worst case supply current delta between temperature extremes was approximately 4mA.

6.3.5 Input Clamp Diode Voltage (VIC)

The input clamp diode voltage exhibited excellent linearity over temperature as expected(See Figure 6.8). Again, this is due to the linear proportionality of P-N junction voltage to temperature. The average VIC measurement was -675mV at -55°C which increased to -500mV at +125°C, an approximate 1mV/°C slope. All values over the temperature range were well within the maximum specified limit of -1.5V.

6.3.6 Output Short Circuit Current (IOS)

By convention, current into the device is considered positive. Therefore, the negative IOS current is a current sourced by the device.

The curves for VOH (shown in Figure 6.5b) and IOS (shown in Figure 6.9), illustrate the direct relationship between output voltage and output short circuit current with respect to temperature. Both sets of curves are similar in their general trend and shape. The average short circuit current at -55°C is -23.5mA and increases to -32mA at +125°C, slightly in the low end of the -20mA to -90mA specified range and below the -40mA typical as set forth by the vendor.

6.3.7 Input/Output Pin Capacitance

Table 6.4 Vendor H Min, Avg, and Max Pin Capacitance

Pin	Min	Avg	Max	Typical Value	Unit
A0-A10	3.9	5.9	6.4	5	pf
INIT	6.0	6.1	6.2	5	pf
E/Es	6.4	6.6	6.8	5	pf
CP	3.8	3.9	4.1	5	pf
O1-O8	13.6	15.2	18.5	12	pf

6.4 AC Parameters

Of the fifteen devices whose AC parameters were characterized serial numbers 1 thru 10 were characterized in the asynchronous or normal mode of operation and the remaining devices, serial numbers 11 thru 15, were programmed in the synchronous mode. A list of the AC parameters that were characterized is given in Table 6.5 below.

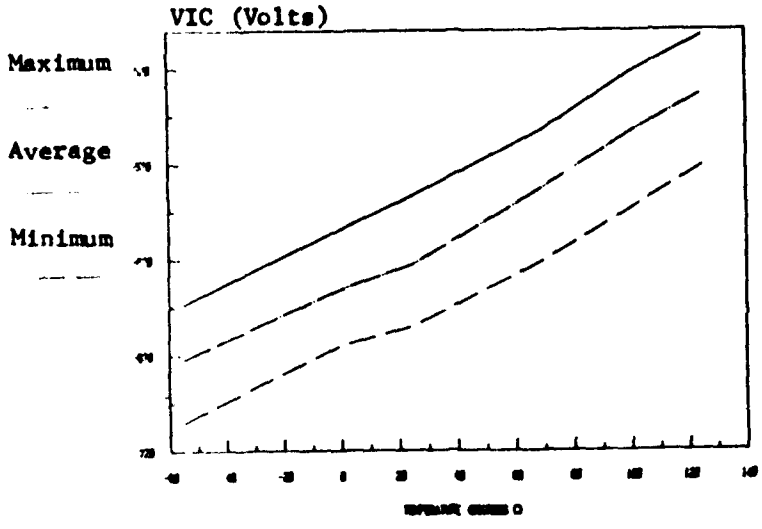


Figure 6.8 Input Clamp Diode Voltage (VIC)

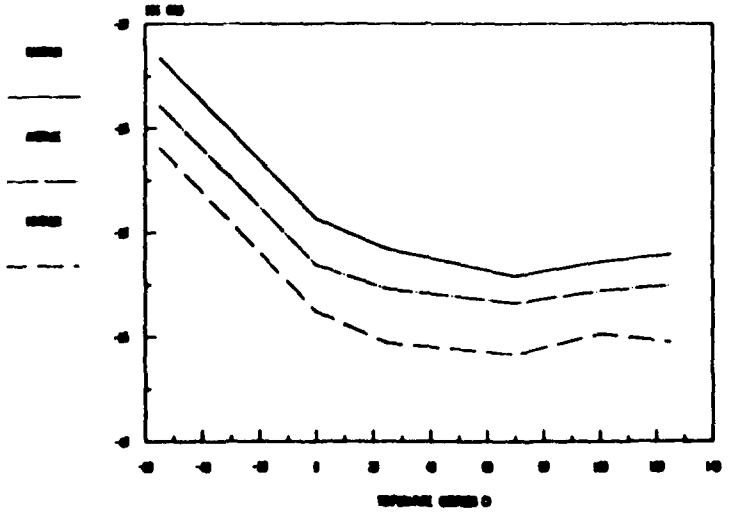


Figure 6.9 Output Short Circuit Current (IOS)

Table 6.5 Vendor Limits for AC Parameters

PARAMETER	SYMBOL	LIMIT		
		MIN	MAX	UNITS
Clock pulse width low	TCLCH	20	---	nsec
Clock pulse width high	TCHCL	20	---	nsec
Address to clock set-up time	TAVCL	45	---	nsec
Enable to clock set-up time	TEXCH	15	---	nsec
Address to clock hold time	TCHAX	0	---	nsec
Enable to clock hold time	TCHEX*	5	---	nsec
Clock high to data valid	TCHDV	---	30	nsec
Enable low to output active	TELQX	---	30	nsec

*Synchronous mode parameters only

6.4.1 Clock Pulse Width Low and High (TCLCH and TCHCL)

The general trend for both TCLCH and TCHCL was decreasing pulse widths with increasing temperature i.e.; the maximum operating frequency increased with temperature and VCC(See Figure 6.10 and 6.11). Some minor failures occurred at the worst case conditions of -55°C and VCC=4.25V with clock pulse low measurements of 22 nsec. Since these devices were screened to 883B, class C, the operating range for VCC is 4.75V to 5.25V only. In that range the worst case condition (4.75V at -55°C) yielded a minimum clock pulse width of 18 nsec which is below the vendors specified minimum of 20 nsec.

6.4.2 Address to Clock Set-up Time (TAVCH)

The required time for an address to be stable before the clock pulse can be applied is the address to clock set-up time. The general trend for this parameter was for decreasing set-up time with increasing temperature and VCC(Figure 6.12). The vendor specified minimum of 45 nsec is more than adequate with worst case measurements of 30 nsec being made at -55°C and 4.25V VCC down to a minimum of 16.5 nsec for VCC=5.25V at 25°C.

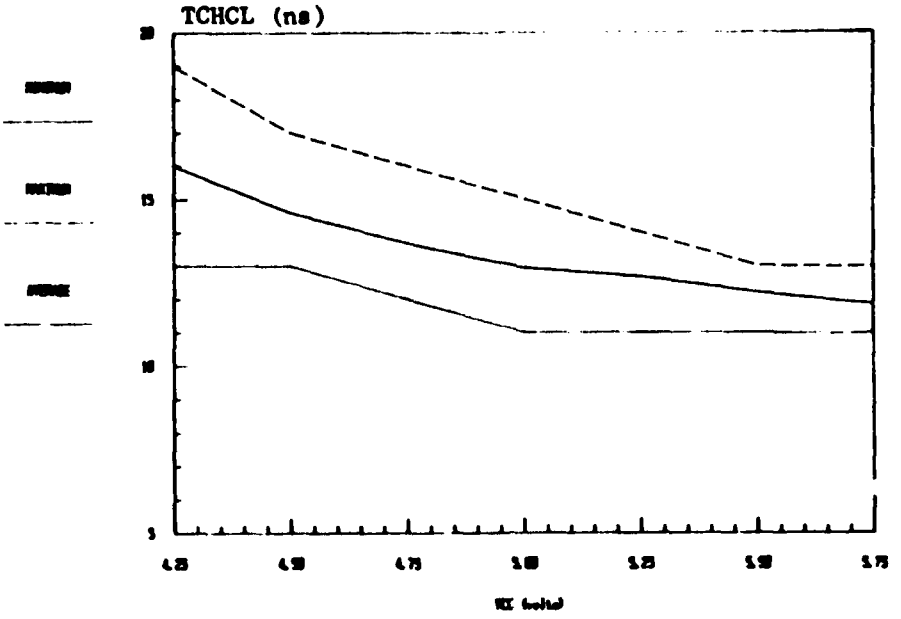


Figure 6.10a Vendor H - Clock Pulse Width High vs. VCC (Temp.=25°C)

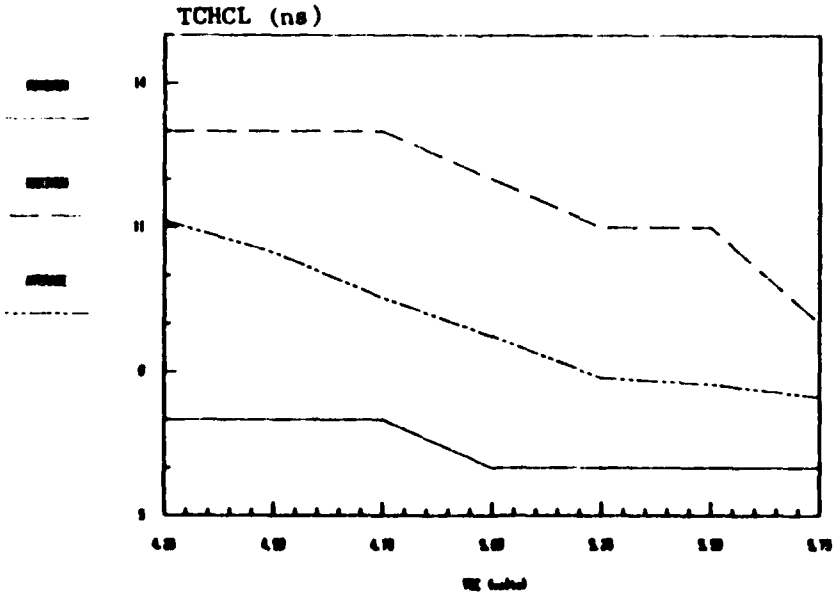


Figure 6.10b Vendor H - Clock Pulse Width High vs. VCC (Temp.=125°C)

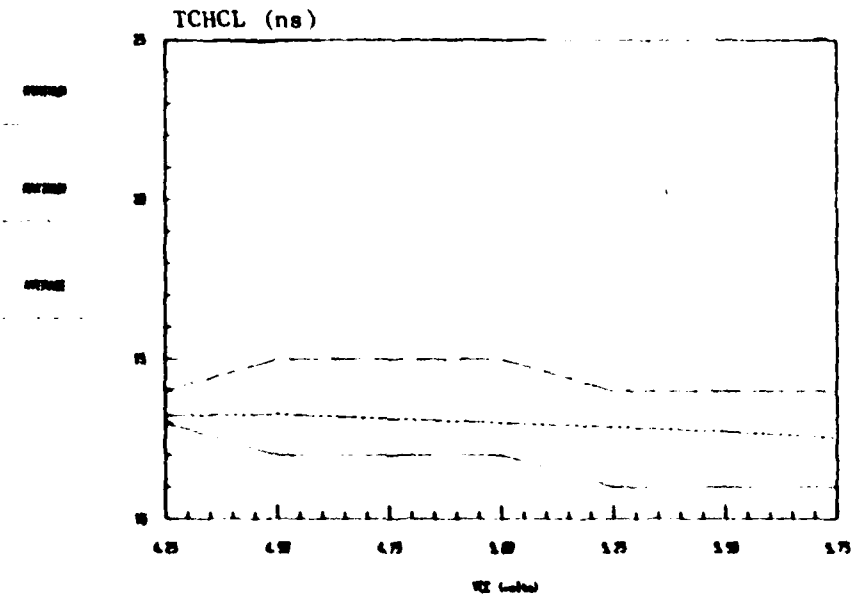


Figure 6.10c Vendor H - Clock Pulse Width High vs. VCC (Temp.=-55°C)

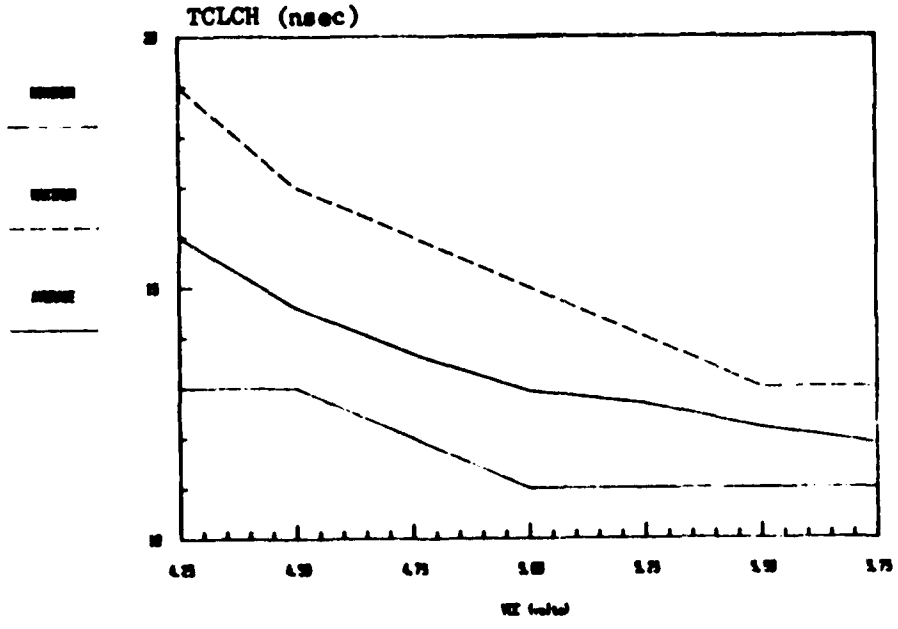


Figure 6.11a Vendor H - Clock Pulse Width Low vs. VCC (Temp.=25°C)

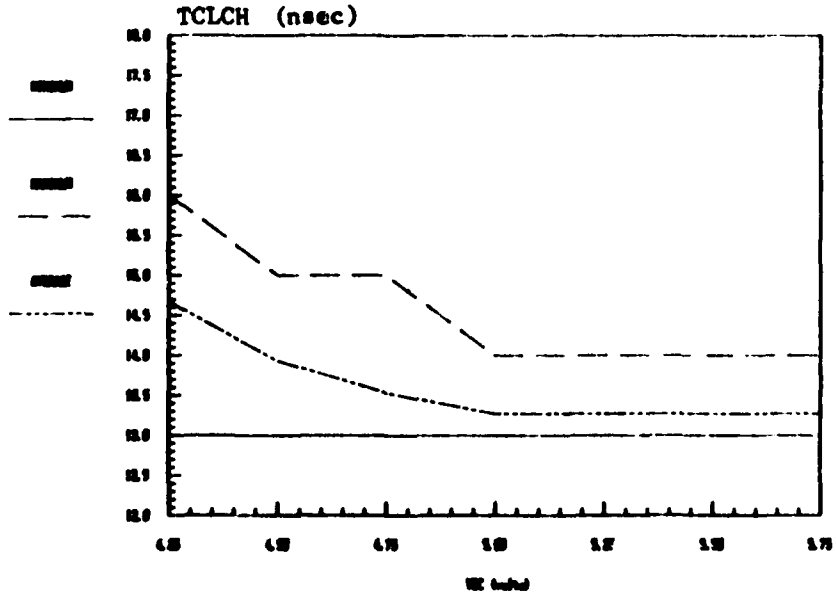


Figure 6.11b Vendor H - Clock Pulse Width Low vs. VCC (Temp.=125°C)

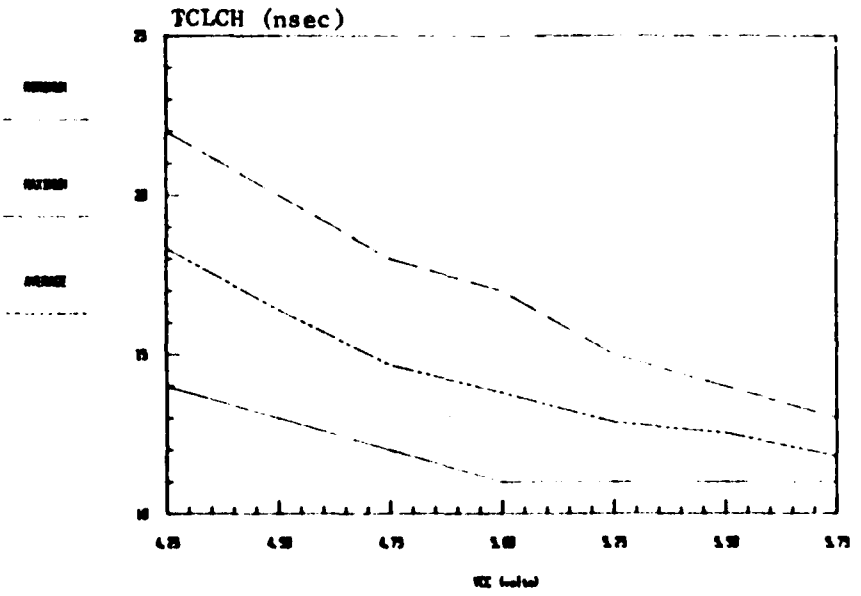


Figure 6.11c Vendor H - Clock Pulse Width Low vs. VCC (Temp.=-55°C)

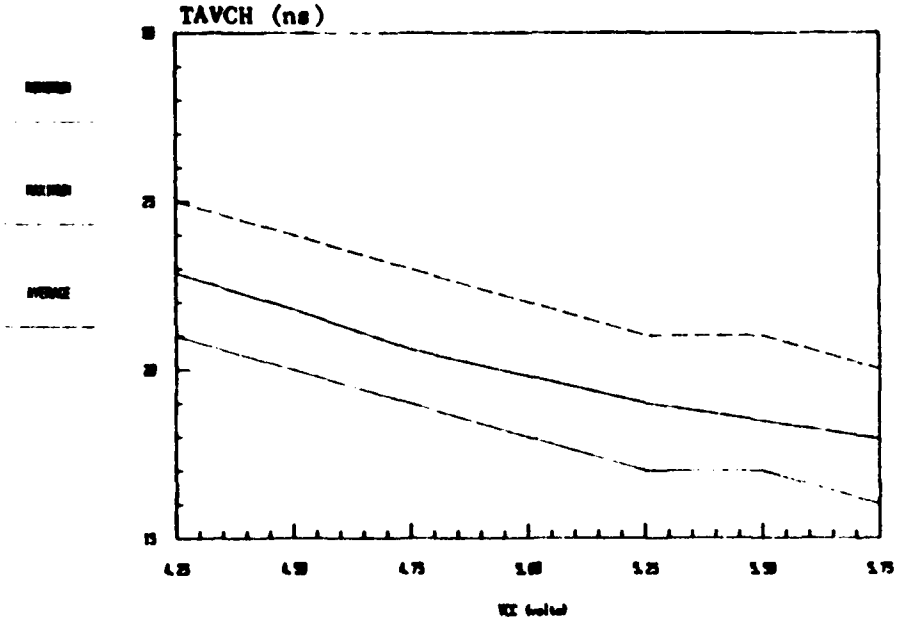


Figure 6.12a Vendor H - Address to Clock Setup Time (Temp.=25°C)

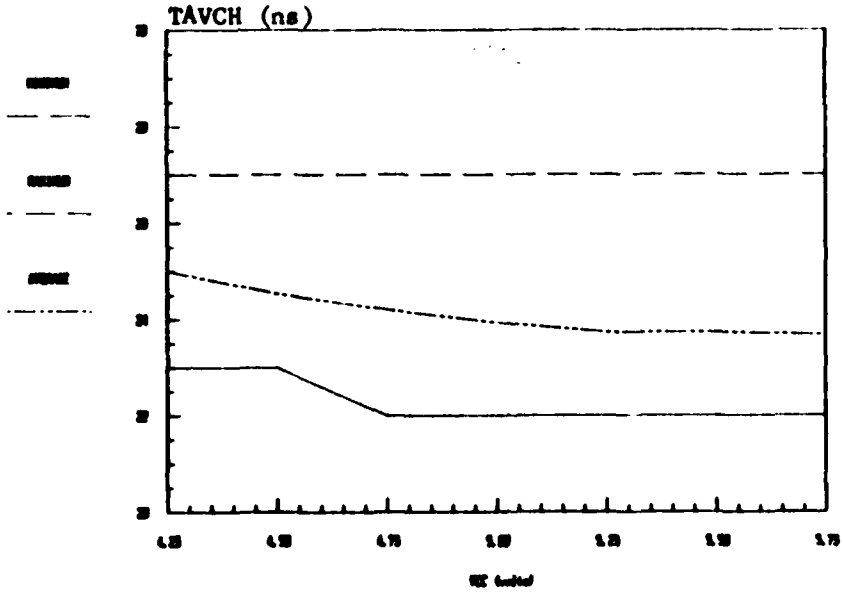


Figure 6.12b Vendor H - Address To Clock Setup Time (Temp.=125°C)

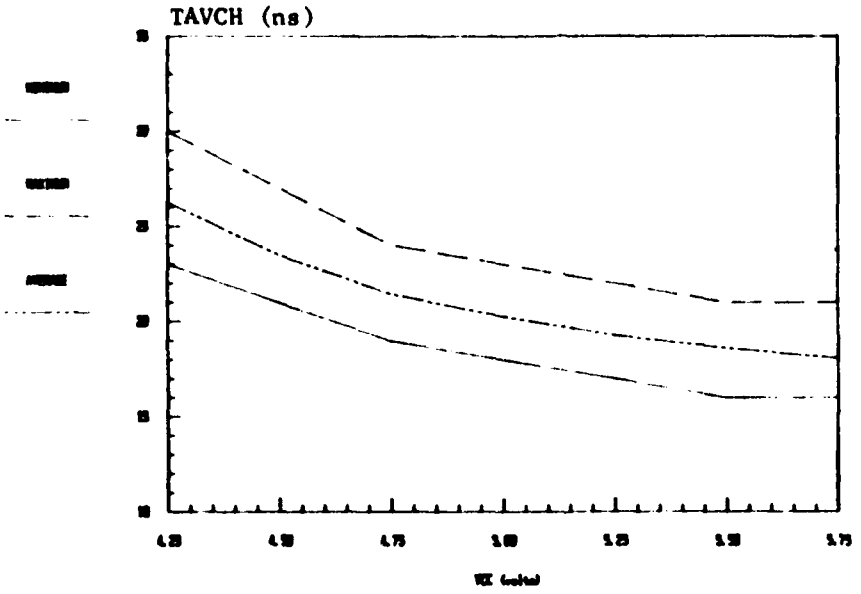


Figure 6.12c Vendor H - Address to Clock Setup Time vs. VCC (Temp.=-55°C)

6.4.3 Clock to Address Hold Time (TCHAX)

The total variation between minimum and maximum TCHAX measurements was only 4 nsec worst case across the temperature and VCC range(See Figure 6.13). Average values ranged from -6.5 nsec at -55°C and nominal VCC (5.0V) to -12 nsec at +125°C. At lower temperatures , -55°C to 25°C, the hold times decreased with increasing VCC. This may be attributed to the fact that hold time is a function of the charge/discharge time of internal circuit nodes. Stiffer driving currents (due to higher supply voltage) tend to decrease these charge/discharge times. At 125°C , however, higher internal resistances tend to dominate thereby increasing charge/discharge times and therefore hold times. All values were well below the 0 nsec minimum as specified by the vendor.

6.4.4 Enable to Clock Set-up Time (TEXCH)

This parameter applies to the synchronous mode of operation only and is the minimum time the enable signal must be present before the clock transition occurs. The range of values over temperature was 6 nsec to 11 nsec, worst case minimum to worst case maximum(Figure 6.14). The average values remain relatively constant over temperature but decrease slightly with increasing VCC. All values, again, were well below the vendor specified minimum of 15 nsec. Referring to the graphs of TEXCH in Figure 6.14, it is significant to note that the plots' step-like response is a result of the measurement deltas being close to and in some cases within, the resolution of the S-3270 Test System. Step type transitions may not necessarily be the response of the device but may instead be a function of the tester.

6.4.5 Clock to Enable Hold Time (TCHEX)

TCHEX is also a synchronous function only and exhibits a very confined response to temperature and VCC. The trend for average values is for increasing hold time with increasing VCC(See Figure 6.15). Worst case average values of -6 nsec at -55°C and 4.25V VCC to -1.5 nsec at 25 C and 5.75 volts VCC are comfortably below the vendor specified minimum of 5 nsec.

6.4.6 Clock High to Data Valid (TCHDV)

Clock high to data valid is the delay time through the output register flip-flops, and exhibits a response that is fairly typical of most bi-polar MSI devices. The parameter decreases at a relatively linear rate with increasing VCC. Temperature variations affect the

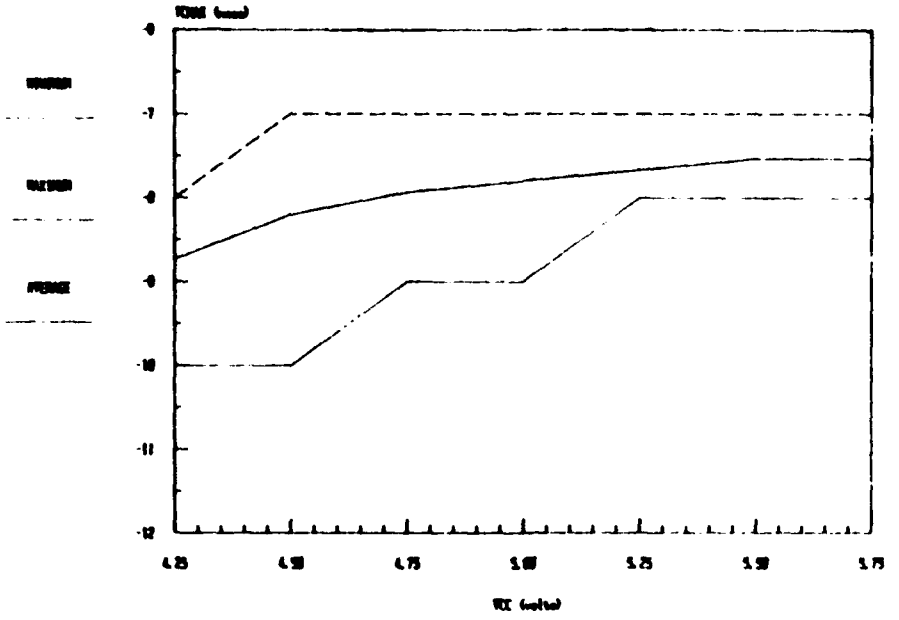


Figure 6.13a Vendor H - Clock to Address Hold Time vs. VCC (Temp.=25°C)

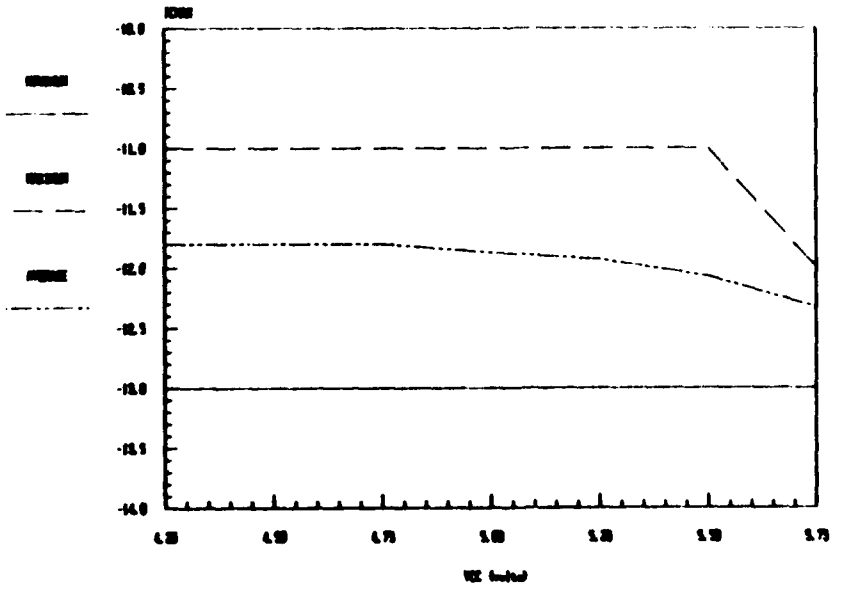


Figure 6.13b Vendor H - Clock to Address Hold Time vs. VCC (Temp.=125°C)

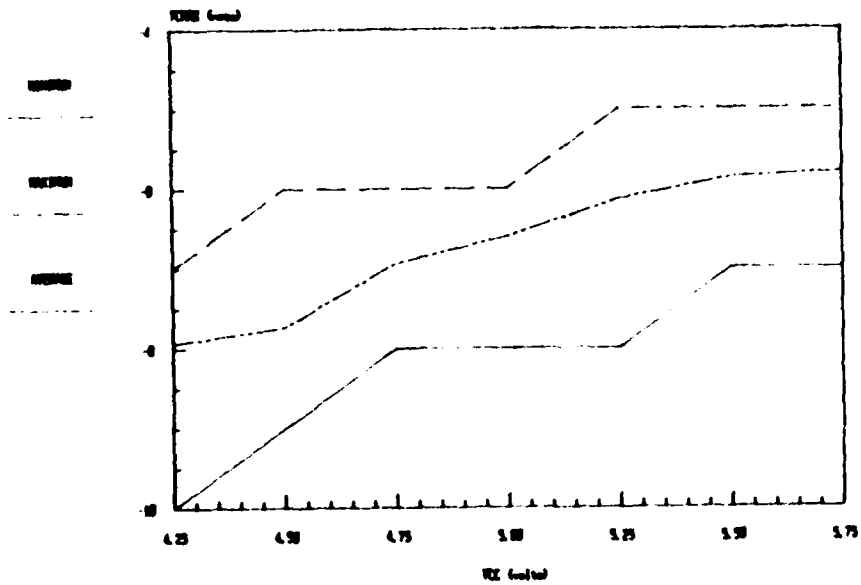


Figure 6.13c Vendor H - Clock to Address Hold Time vs. VCC (Temp.=-55°C)

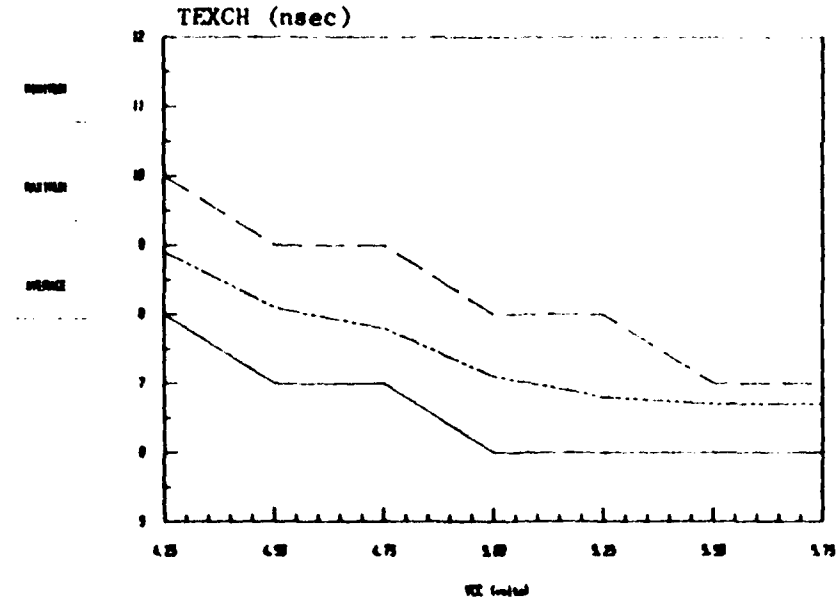


Figure 6.14a Vendor H - Enable to Clock Setup Time vs. VCC (Temp.=25°C)

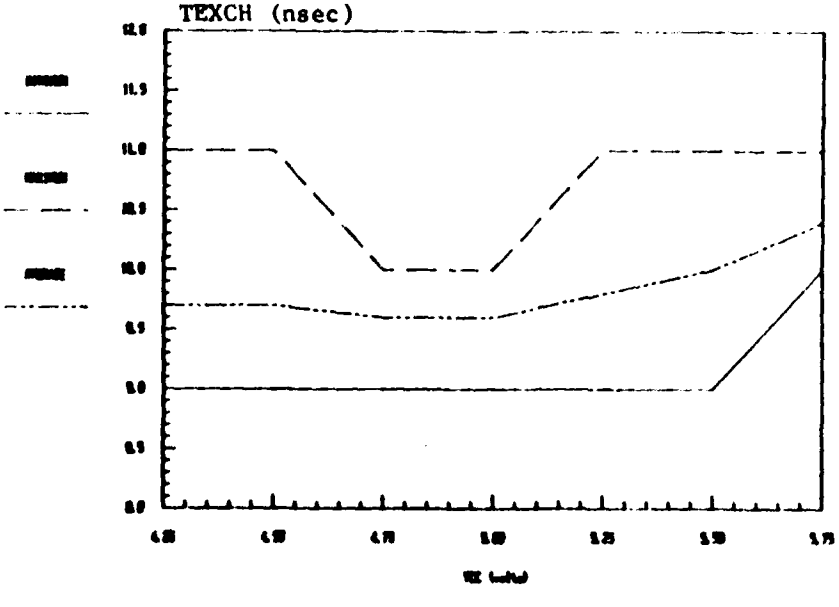


Figure 6.14b Vendor H - Enable to Clock Setup Time vs. VCC (Temp.=125°C)

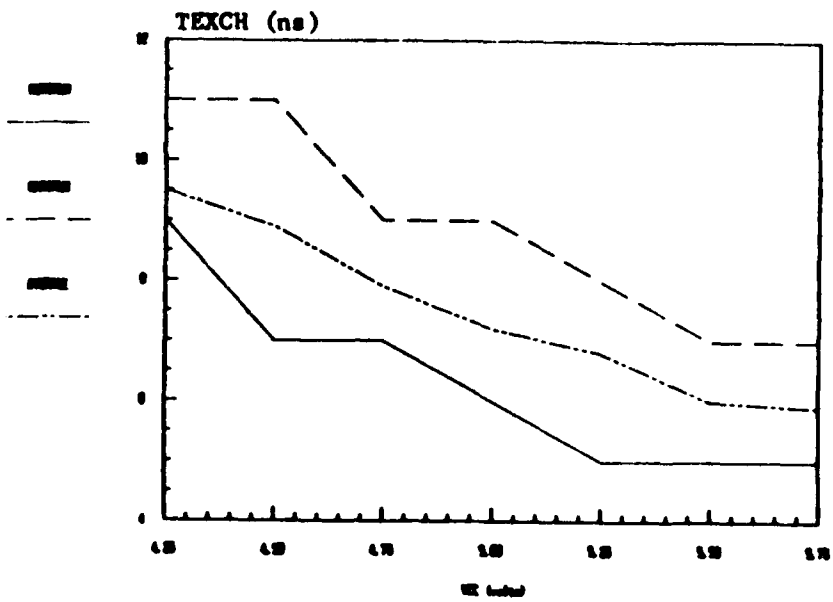


Figure 6.14c Vendor H - Enable to Clock Setup Time vs. VCC (Temp.=-55°C)

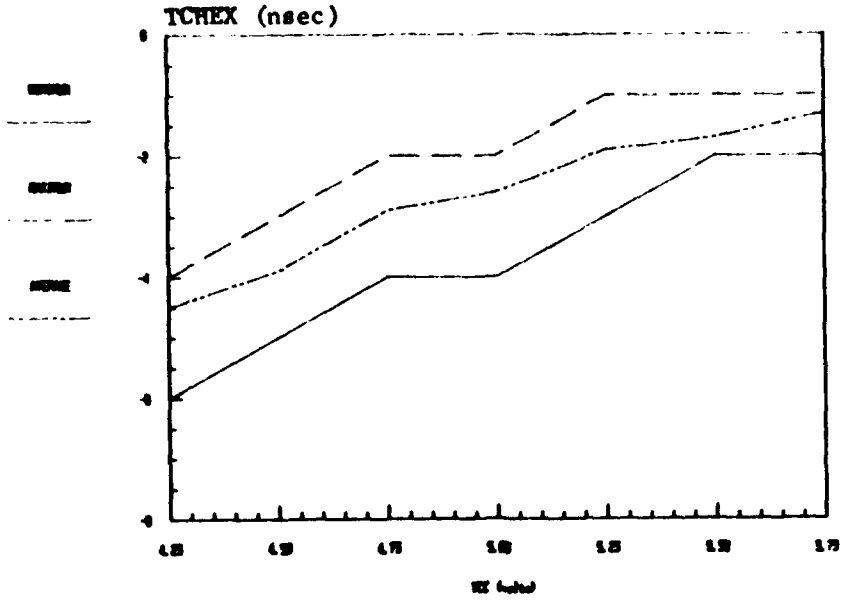


Figure 6.15a Vendor H - Clock to Enable Hold Time vs. VCC (Temp.=25°C)

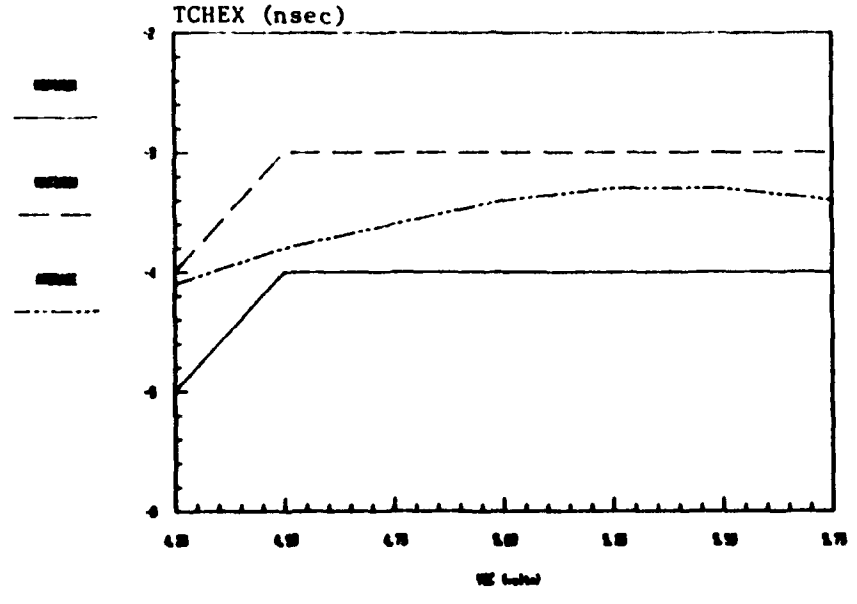


Figure 6.15b Vendor H - Clock to Enable Hold Time vs. VCC (Temp.=125°C)

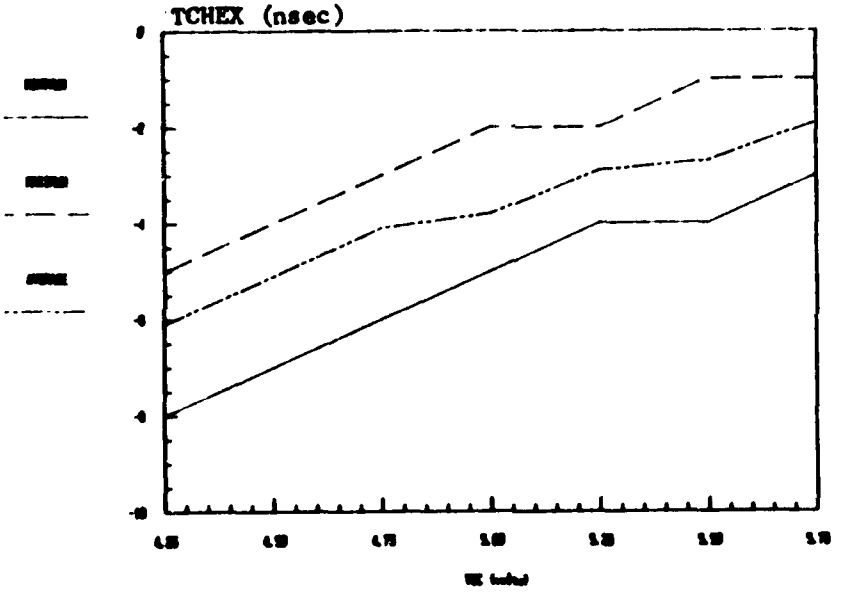


Figure 6.15c Vendor H - Clock to Enable Hold Time vs. VCC (Temp.=-55°C)

response only slightly with a 4 nsec variation in average values over the full military temperature range (See Figure 6.16). The maximum value of 26 nsec at -55°C and 4.25V VCC is less than the 30 nsec specified maximum.

6.4.7 Output Buffer Turn-on Time (TELQX) - Asynchronous Mode

Output buffer turn-on time is a delay through the output buffer circuitry and is very similar to TCHDV as discussed above. Over the full temperature range TELQX exhibits a bath-tub type curve (see Figures 6.17a, b, and c); i.e. decreasing values from -55°C to 25°C, flat to 100°C and slightly increasing to +125°C. All devices were at or below the vendor's limit for TELQX within the specified VCC operating range of 4.5V to 5.5V. All values decrease rather linearly with increasing VCC. Average values ranged from 28 nsec at 4.5V VCC and -55°C to 22 nsec at +125°C and 5.5V VCC.

6.4.8 Output Disable Time(TEHQZ)

Output disable time is summarized in Table 6.6 below.

Table 6.6a Output Disable Time - Output initially at VOL

S/N	TEHQZ	Units
1	26	nsec
2	28	
3	28	
4	27	
5	30	
6	30	
7	32	
8	32	
9	30	
10	28	
11	20	
12	20	
13	20	
14	20	
15	20	

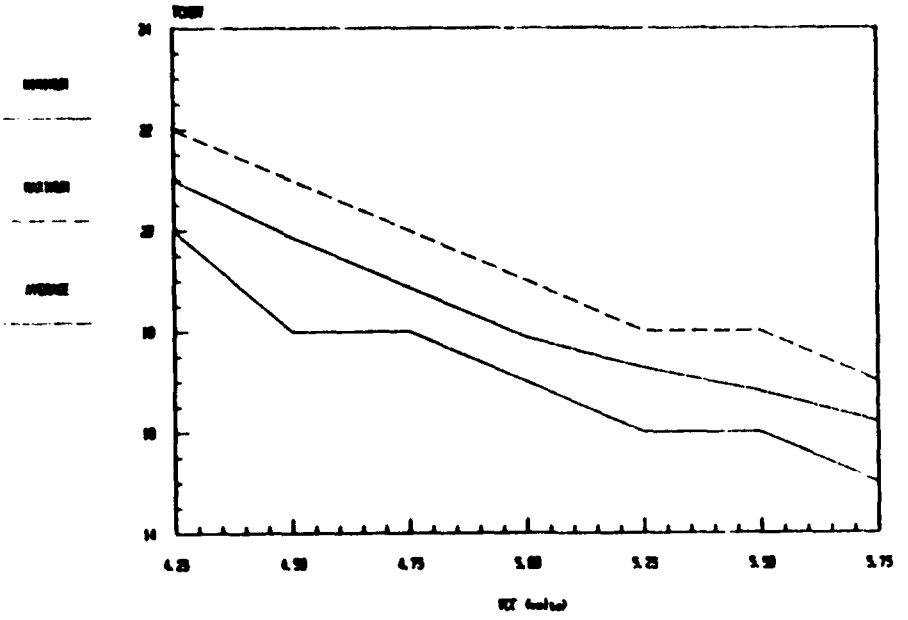


Figure 6.16a Vendor H - Clock High to Data Valid Time vs. VCC (Temp.=25°C)

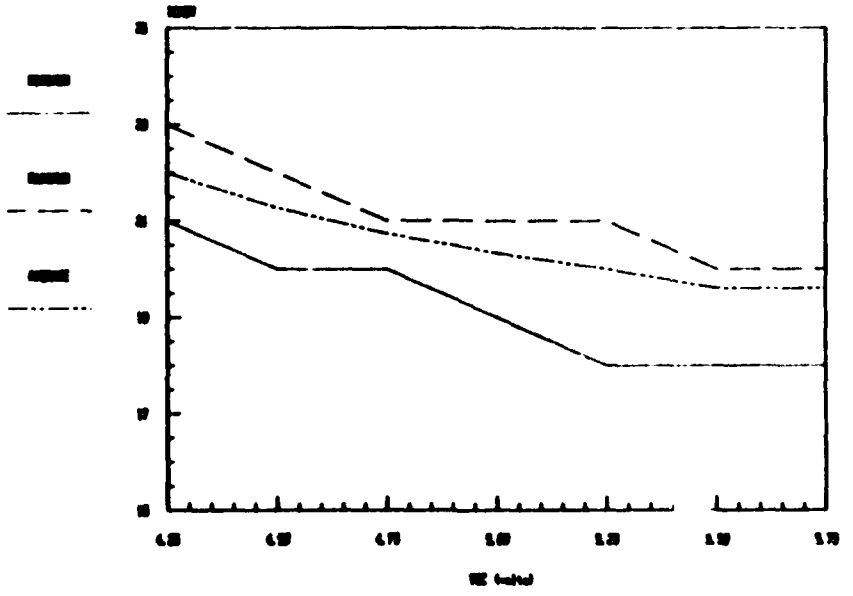


Figure 6.16b Vendor H - Clock High to Data Valid Time vs. VCC (Temp.=125°C)

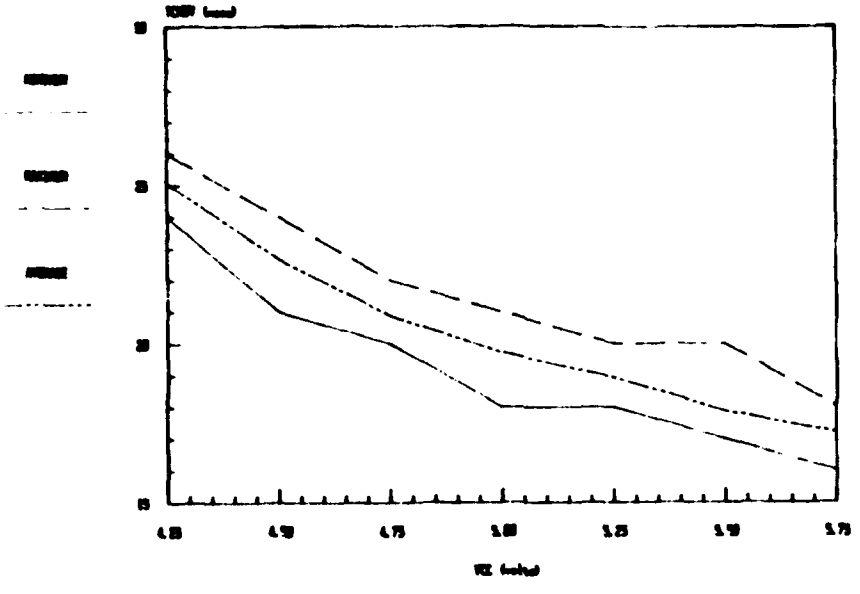


Figure 6.16c Vendor H - Clock High to Data Valid Time vs. VCC (Temp.=-55°C)

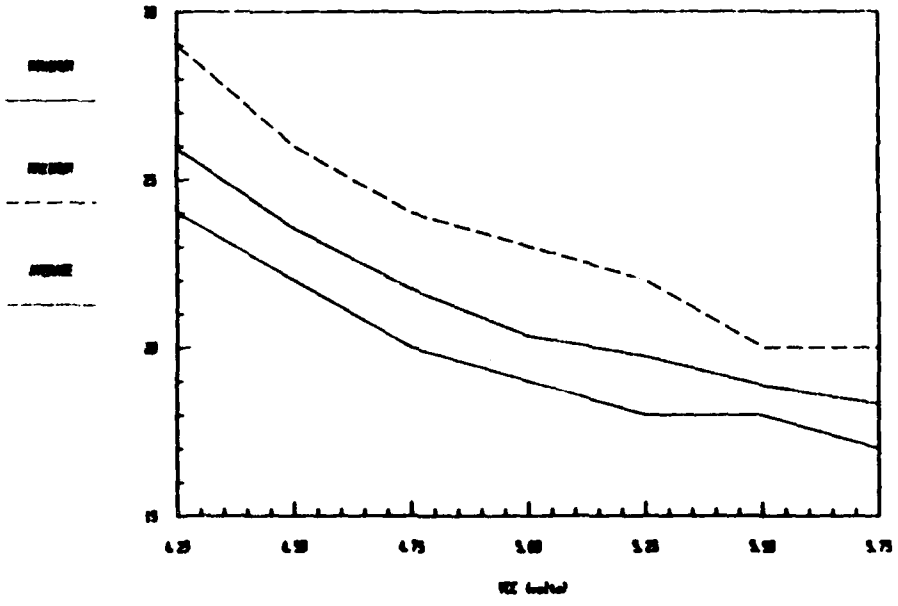


Figure 6.17a Vendor H - Output Buffer Turn-on Time vs. VCC (Temp.=25°C)

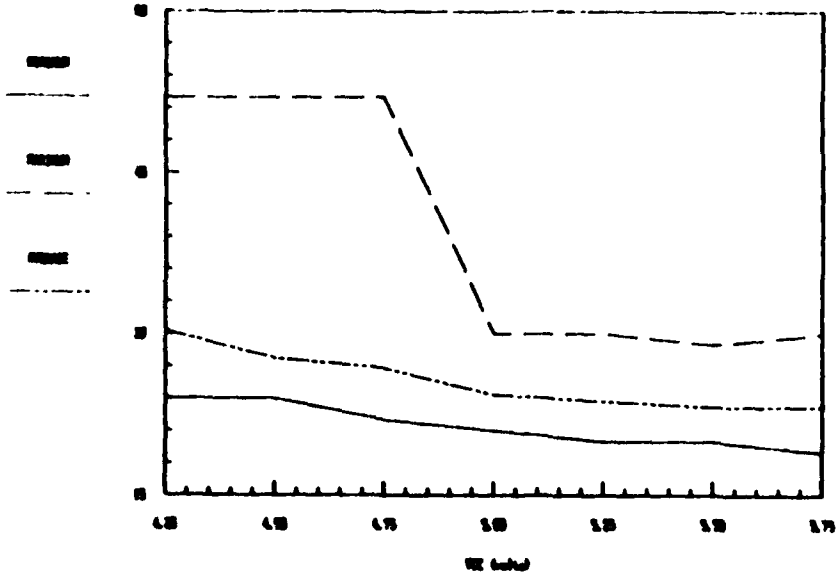


Figure 6.17b Vendor H - Output Buffer Turn-on Time vs. VCC (Temp.=125°C)

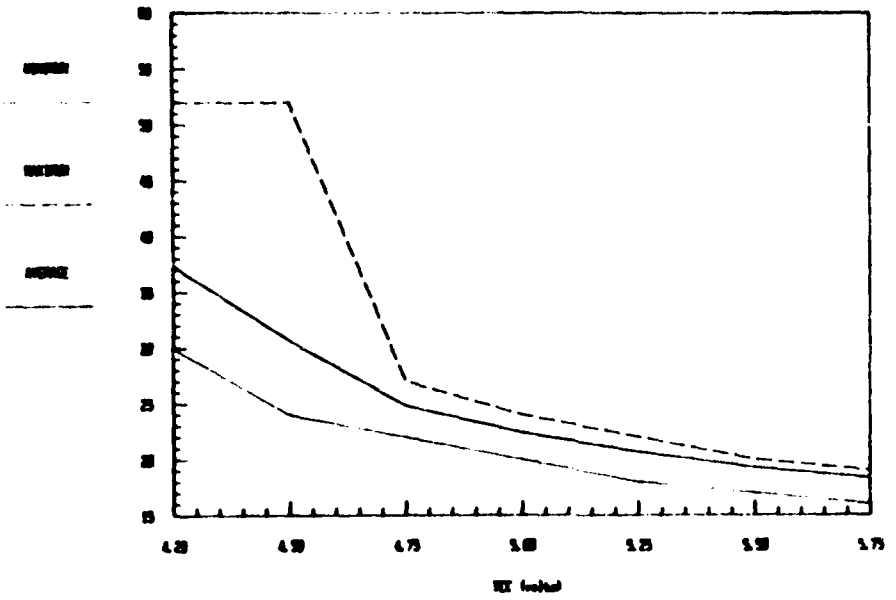


Figure 6.17c Vendor H - Output Buffer Turn-on Time vs. VCC (Temp.=-55°C)

Table 6.6b Output Disable Time - Output initially at VOH

S/N	TEHQZ	Units
1	24	nsec
2	23	
3	25	
4	23	
5	25	
6	25	
7	26	
8	25	
9	25	
10	24	
11	26	
12	26	
13	27	
14	26	
15	27	

6.5 AC Characterization Summary

The AMD 27S45 performed well during AC characterization despite the fact that it was not an 883 device. It operated beyond the manufacturer's specified range for both VCC and temperature and in all but one instance, within the vendor's specified limits. The values and trends exhibited by the 27S45 were typical of bi-polar devices of similar size and complexity. The ability to be programmed for synchronous or asynchronous operation along with the initialization function gives the device added flexibility and desirability over more standard ROM devices.

7. 16K-STATIC RAM

7.1 Introduction (16K X 1 Static RAMs)

The INMOS IMS1400M and Integrated Device Technology(IDT) IDT6167L85 are 16,384 bit high speed Static RAMs organized as 16K X 1, featuring access times of 70nS and 85nS respectively. Other features include chip enable (CE) - controlled low-power standby mode and single +5V operation. N-MOS technology was used by Inmos while IDT used CMOS.

Military grade(883B) devices from each vendor were provided for the characterization. Access times of the devices provided by Inmos and IDT were 70nsec and 85nsec respectively. Vendor I refers to Inmos and Vendor J refers to IDT. Table 7.1 summarizes the device part number, date code, access time, and lot quantity.

Table 7.1 Devices Provided for Characterization

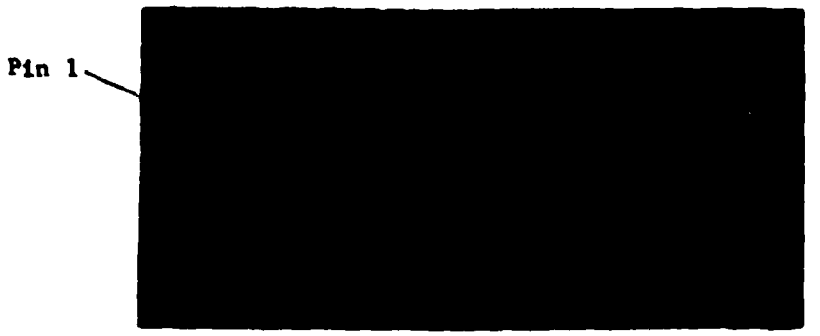
Vendor	Part No.	Access Time	Date Code	Quantity
I	IMS1400M	70nS	8227	23
J	IDT6167L85	85nS	8243	20

Table 7.2 provides the chip dimensions for the two vendors. Micro-photographs of a die from each vendor are shown in Figure 7.1. Both photographs are to the same scale so that a visual size comparison can be made.

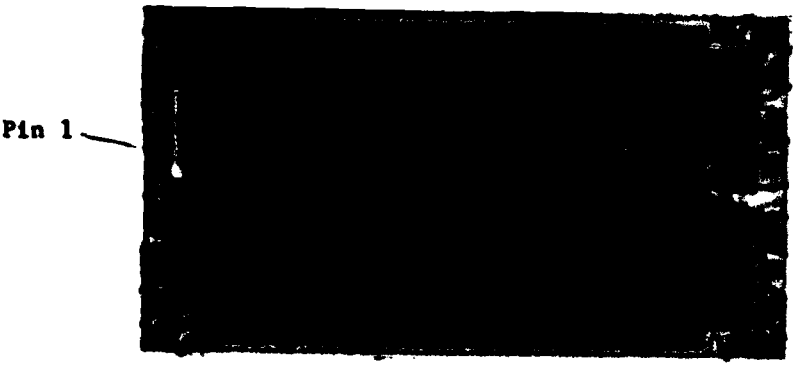
Table 7.2 16Kx1 Static RAM Chip Dimensions

Vendor	Length (mm)	Width (mm)	Area (sq mm)
I	6.46	3.09	19.96
J	6.27	3.30	20.69

The package that was characterized for both vendors is a 20 pin ceramic dual-in-line. The pin configuration for this package is shown in Figure 7.2 for both vendors. At the time of characterization, Vendor I offered a 70nS device while Vendor J offered four versions with access times ranging from 55nS to 100nS. All device inputs and outputs for both vendors are TTL compatible. Fully static circuitry is used which requires no clocks or refreshing and provides equal access and cycle times.



Vendor I



Vendor J

Figure 7.1 Die Photos - 16Kx1 Static RAMs (14.84X)

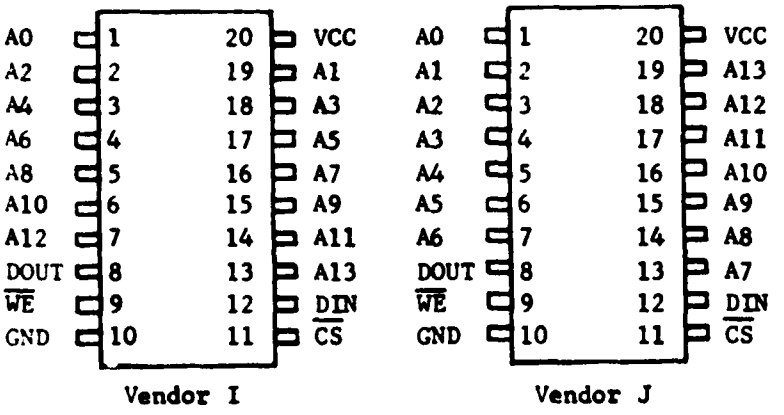


Figure 7.2 16Kx1 Static RAM Pin Configuration

7.2 Incoming Test

All devices from each vendor passed the incoming test.

7.3 DC Parameters

The DC parameters and test conditions specified by the two manufacturers are listed in Table 7.3. All parameters except input thresholds were measured at -55, 0, 25, 70, 100, and 125°C.

Table 7.3 Vendor Specified DC Parameters

Symbol	Parameter	Vendor I Min	Vendor I Max	Vendor J Min	Vendor J Max	Unit
VCC	Supply Voltage	4.5	5.5	4.5	5.5	V
ICC1	Supply Current (Static - DC)	-	90	-	50	mA
ICC2	Supply Current (Dynamic - AC)	-	120	-	50	mA
ICC3	Supply Current (Standby)	-	30	-	20	mA
IIL, IIH	Input Leakage Current	-10	-10	-	5	uA
IOLZ, IOHZ	Output Leakage Current	-50	50	-	5	uA
VIL	Low Level Input Voltage	-2.0	0.8	-.5	0.8	V
VIH	High Level Input Voltage	2.4	6.0	2.2	6.0	V
VOL	Low Level Output Voltage	-	0.4 IOL=16mA	-	0.4 IOL=8mA	V
VOH	High Level Output Voltage	2.4 IOH=-4mA	-	2.4 IOH=-4mA	-	V

7.3.1 Leakage Current

Input Leakage Currents, IIH and IIL, and Output Leakage currents, IOLZ and IOHZ, were well below the manufacturer's specified maximum limits. All were less than 100nA.

7.3.2 Logic Output Voltage (VOH, VOL)

All devices passed the specified VOH limit at the six temperatures. The average of the minimum VOH values are plotted in Figure 7.3. Each vendor specifies the same output current condition (IOH) of -4mA. The plot in Figure 7.3 shows Vendor I with a lower average minimum VOH than Vendor J. VOH for Vendor I tends to decrease with temperature while VOH for Vendor J increases.

A plot of average maximum VOL values for both vendors is shown in Figure 7.4. All devices passed their maximum specified VOL limit for all temperatures. VOL for Vendor J is an average of 100mV less than Vendor A. Both plots in Figure 7.4 illustrate that as temperature increases VOL increases.

7.3.3 Input Logic Level Sensitivity

Access time sensitivity to various input logic levels was determined for 2 devices from both vendors. Three different cases of input logic levels were used:

CASE 1: VIL = 0.8V, VIH = 2.0V
CASE 2: VIL = 0.6V, VIH = 2.4V
CASE 3: VIL = 0.4V, VIH = 3.0V

As the input voltage levels were varied, measurements were made of access time (TAVQV) at 25°C with VCC levels of 4.5V, 5.0V, and 5.5 volts. TAVQV for the three cases of input conditions is given in Table 7.4.

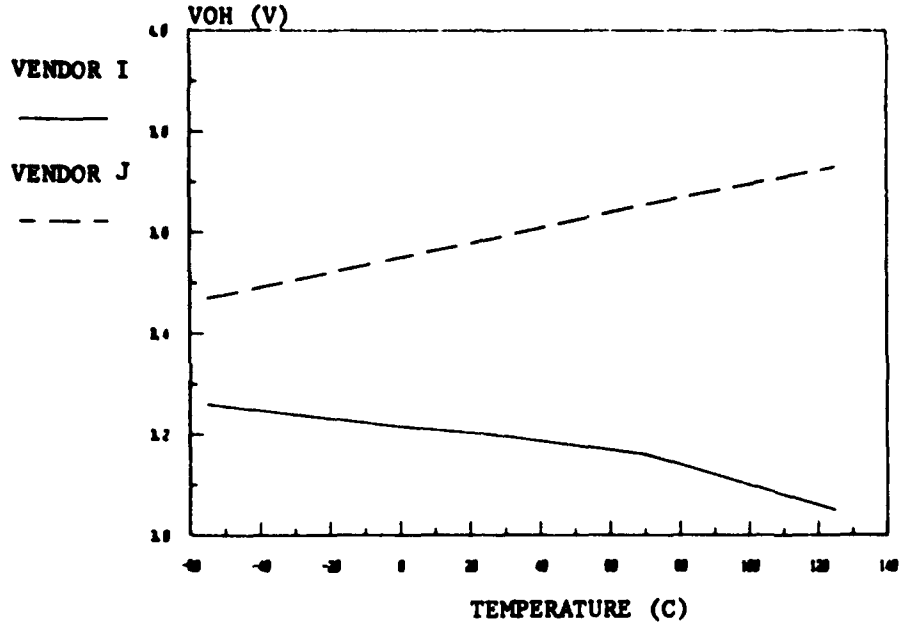


Figure 7.3 Average of Minimum VOH Values

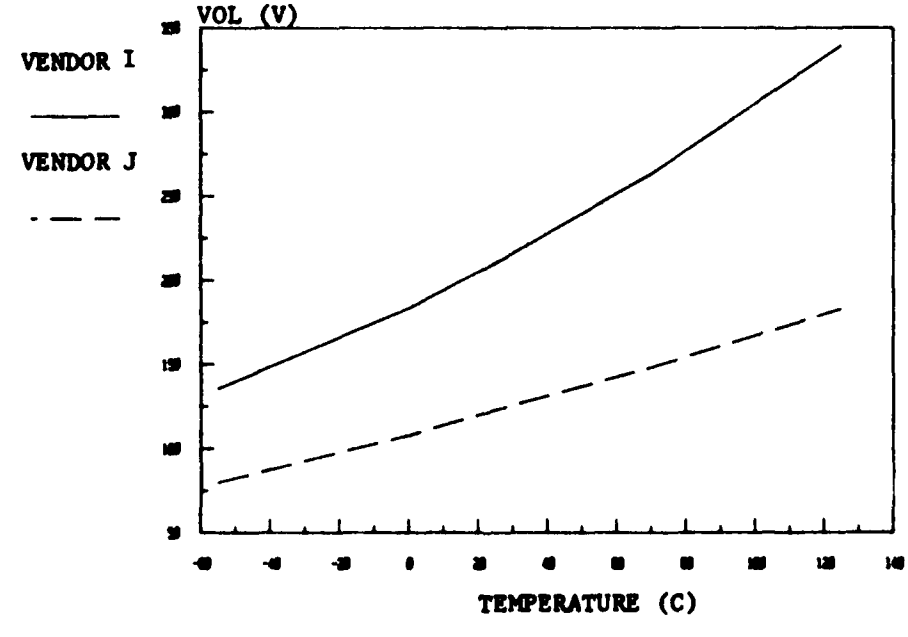


Figure 7.4 Average of Maximum VOL Values

Table 7.4 Access Times for 3 Different Cases of Input Logic Levels at 25°C

Vendor I

S/N	VCC	TAVQV Case 1	TAVQV Case 2	TAVQV Case 3
1	4.5	43.48	43.48	43.48
	5.0	43.48	38.79	38.79
	5.5	43.48	36.45	37.62
5	4.5	38.79	38.79	38.79
	5.0	38.79	35.27	36.45
	5.5	39.96	35.27	36.45

Vendor J

S/N	VCC	TAVQV Case 1	TAVQV Case 2	TAVQV Case 3
1	4.5	39.96	39.96	39.96
	5.0	39.96	36.45	36.45
	5.5	38.79	34.1	34.1
5	4.5	39.96	38.79	39.96
	5.0	38.79	35.27	36.45
	5.5	38.79	32.93	32.93

The data in Table 7.4 shows little sensitivity to the three applied logic level conditions. Vendor I shows a slightly greater shift in access time than Vendor J. At VCC = 5.5V the average change in access time from Case 1 (41.7nS) to Case 2 (35.9nS) is 5.85nS. Vendor J for VCC = 5.5V displays an average shift of 5.27nS from Case 1 to Case 2. Access time decreases slightly for both vendors as VCC increases from 4.5V to 5.5V.

7.3.4 Supply Current (ICC)

The three supply current measurements performed at six temperatures are as follows:

a.) ICC1 - measured in static DC state
b.) ICC2 - measured in active READ/WRITE state
c.) ICC3 - measured during standby

All supply current measurements were well within the manufacturer's specifications. Average values of ICC1 and ICC2 versus temperature are shown in Figures 7.5 and 7.6 respectively. An average of ICC3 versus temperature is shown in Figure 7.7.

7.3.5 Input/Output Pin Capacitance

Capacitance measurements were performed on all pins except VCC and GND for five devices from each vendor. Tables 7.5a and 7.5b indicate the Min, Avg and Max capacitance values per pin along with the specified maximum limits.

The input and output pin capacitance values for both vendors were found to be within the specified maximum limits.

Table 7.5a Vendor I Min, Avg and Max Input/Output Pin Capacitance

Pin	Min	Avg	Max	Limits	Units
A0-A13	1.5	2.0	3.3	4	pf
DOUT	4.8	4.8	4.8	7	pf
WE	2.1	2.1	2.1	4	pf
CS	2	2	2	4	pf
DIN	1.8	1.8	1.8	4	pf

Table 7.5b Vendor J Min, Avg and Max Input/Output Pin Capacitance

Pin	Min	Avg	Max	Limits	Units
A0-A13	2.1	2.5	3.5	5	pf
DOUT	3.4	3.4	3.4	6	pf
WE	3.2	3.2	3.2	5	pf
CS	2.3	2.3	2.3	5	pf
DIN	2.1	2.1	2.1	5	pf

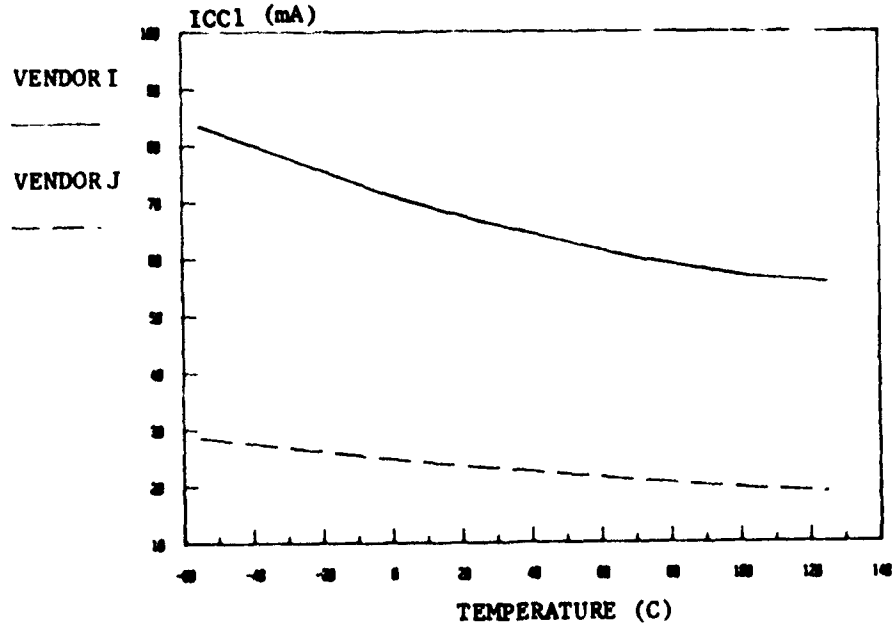


Figure 7.5 Average of ICC1, Static DC Supply Current

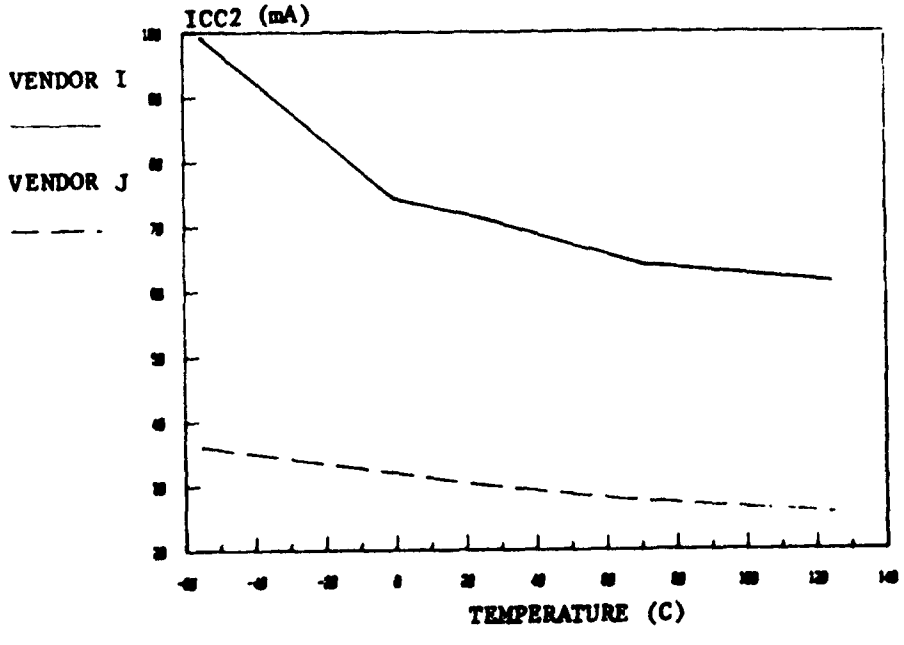


Figure 7.6 Average of ICC2, Active DC Supply Current

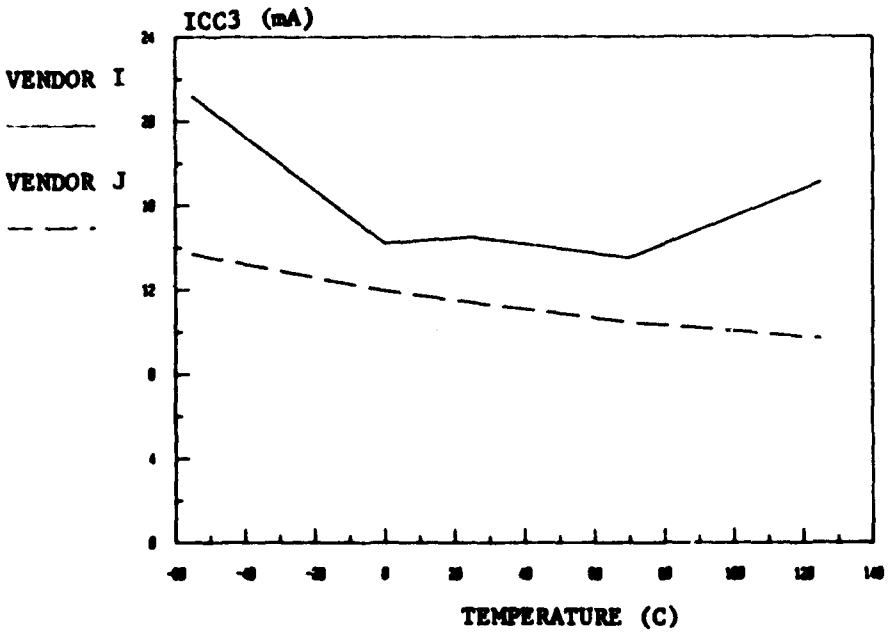


Figure 7.7 Average of ICC3, Standby Supply Current

7.4 AC Characterization

The AC parameters that were characterized and their vendor specified limits are listed in Table 7.6. Refer to Appendix B for timing parameter abbreviations used in this section.

Table 7.6 Vendor Limits for AC Parameters

	Vendor I		Vendor J	
	Min	Max	Min	Max
TAVQV	-	65nS	-	85nS
TELQV	-	70nS	-	85nS
TAVWL	8nS	-	0	-
TAXQX	0nS	-	5	-

7.4.1 Vendor I AC Parameters

The four timing parameters characterized were TAVQV, TELQV, TAVWL, and TAXQX.

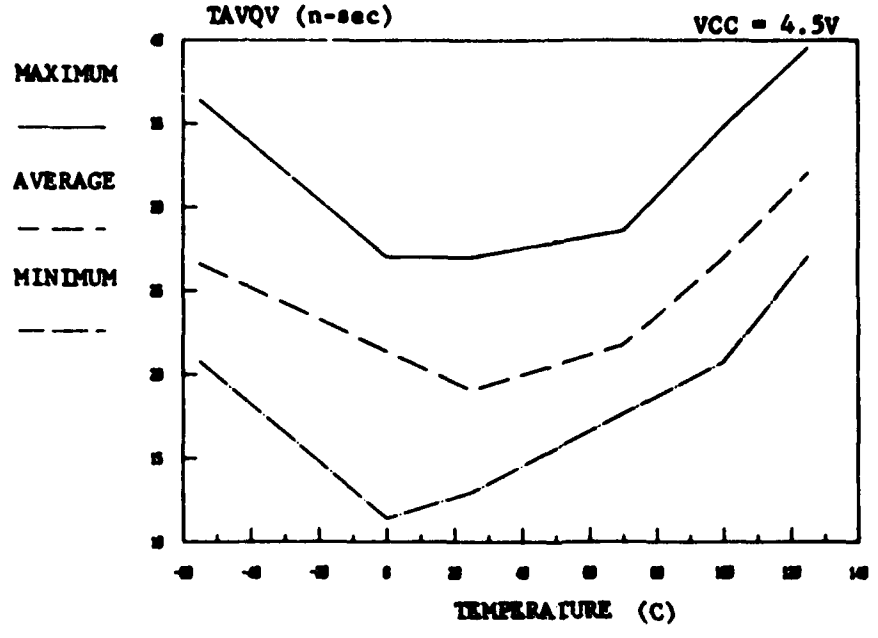
7.4.1.1 Address and Chip Enable Access Time

Plots of Address Access Time (TAVQV) for Vendor I at -55, 0, 25, 70, 100, and 125°C are shown in Figure 7.8. The plot of TAVQV for VCC = 4.5V and 5.5V shows a sensitivity to the two temperature extremes (-55°C, 125°C). At VCC = 5.5V, the high temperature sensitivity is not as pronounced as at 4.5V. The plots show that TAVQV for both VCCs is within the specified limits.

Figure 7.9 shows plots of Chip Enable Access Time (TELQV) versus temperature for the two VCC levels. At 4.5V there is some sensitivity to low temperature. From 0°C to 125°C, TELQV increases from an average of 45nS to 58.5nS. At 5.5V, TELQV is less temperature dependent than at 4.5V. The largest average variation is 4.5nS.

7.4.1.2 Address Setup Time

Address Setup Time (TAVWL) at the six temperatures and two VCC levels is plotted in Figure 7.10. For both levels of VCC, TAVWL increases with an increase of temperature. TAVWL is an average of 4nS higher at 5.5V than at 4.5V.



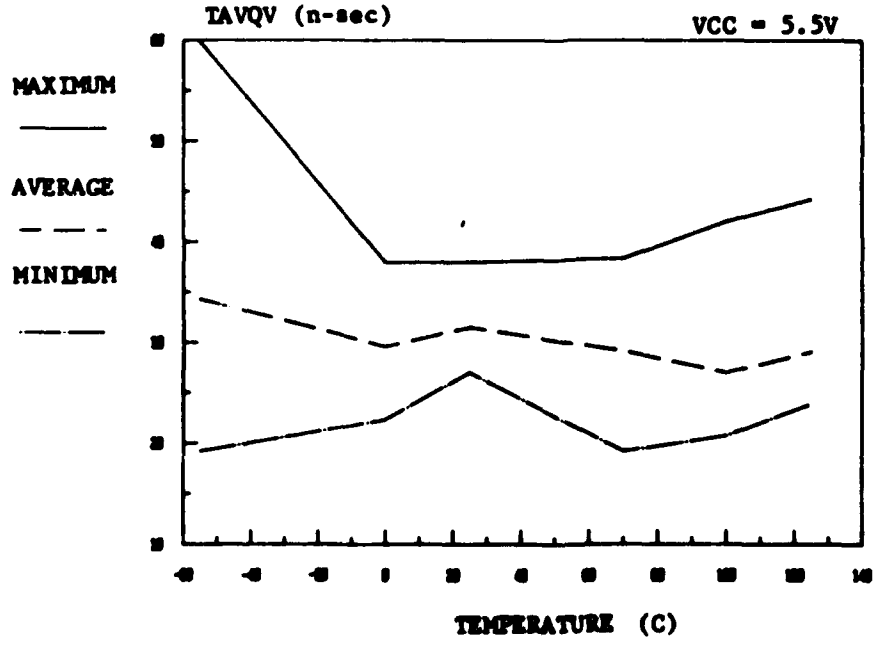
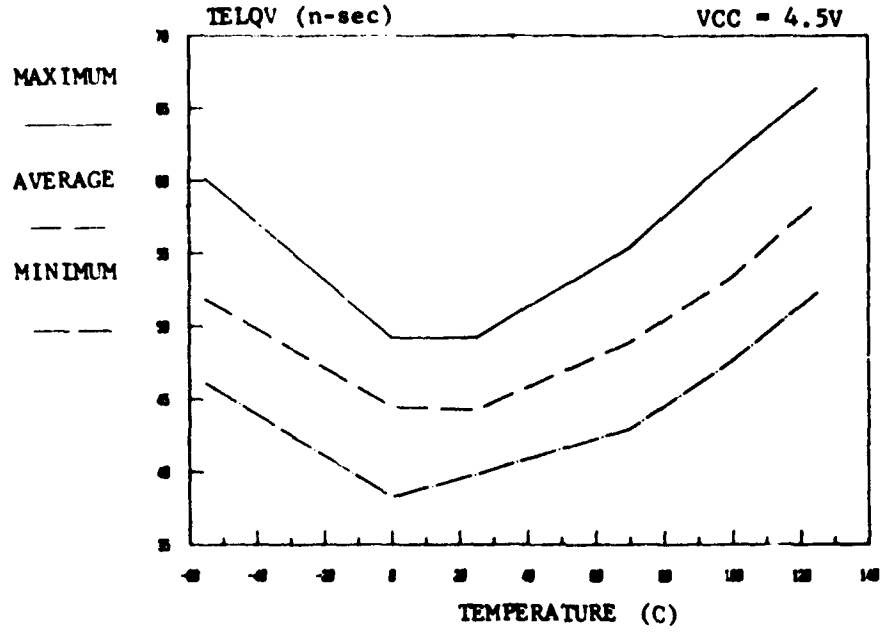


Figure 7.8 Vendor I - Address Access Time vs. Temperature



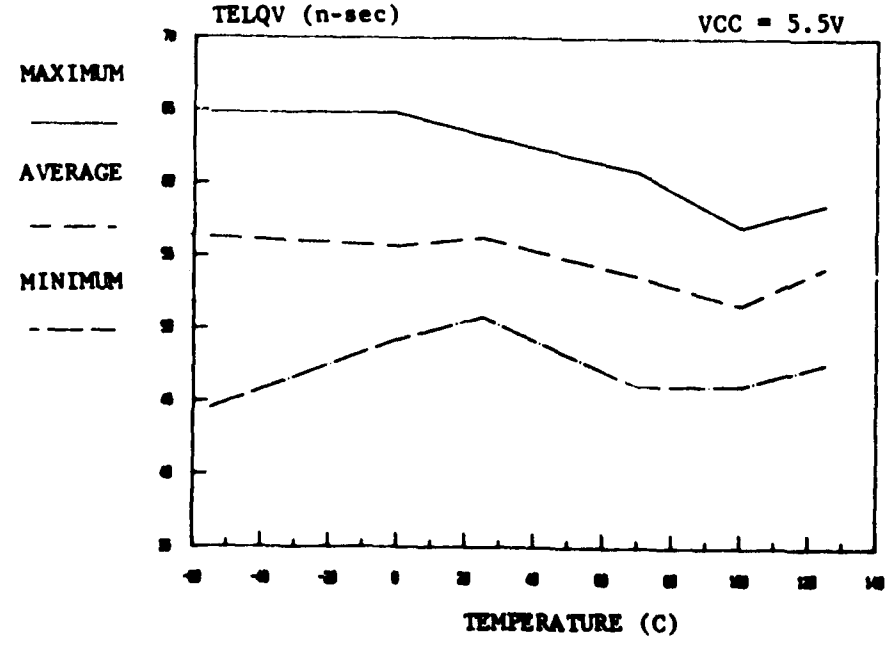
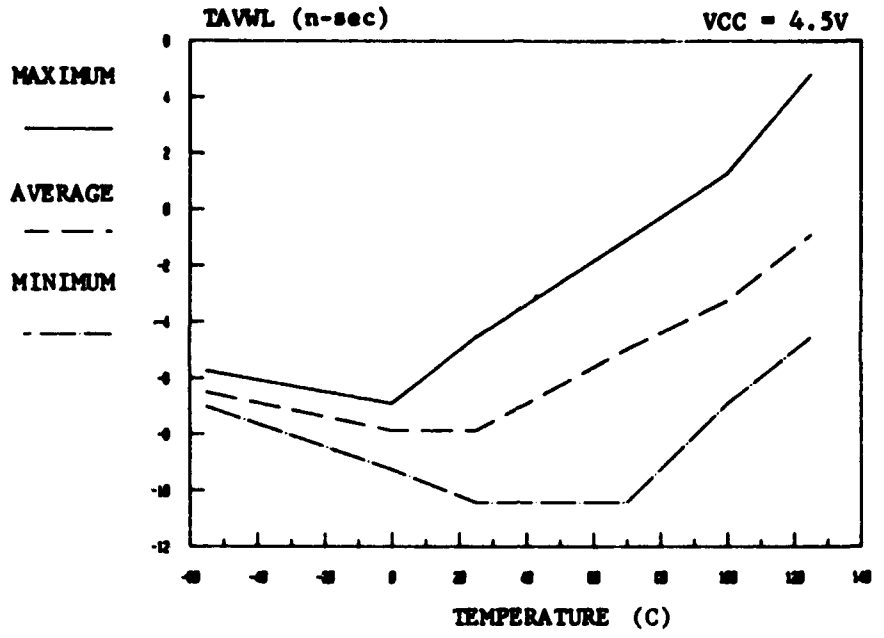


Figure 7.9 Vendor I - Chip Enable Access Time vs. Temperature



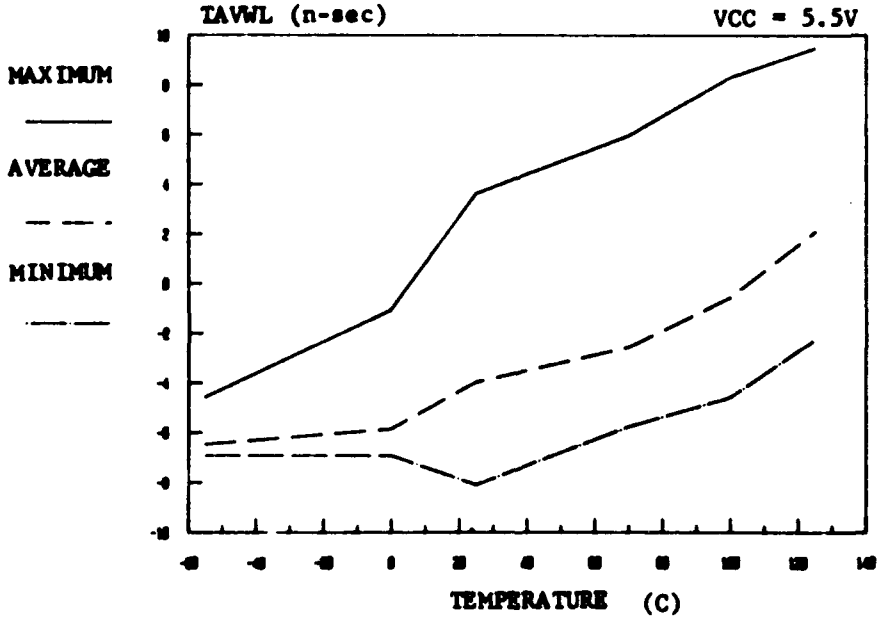


Figure 7.10 Vendor I - Address Setup Time vs. Temperature

7.4.1.3 Address to Invalid Data Output

Plots of Address to Data Invalid (TAXQX) are shown in Figure 7.11. TAXQX increases with temperature for both levels of VCC and is only an average of 2nS higher for VCC = 4.5V. Average TAXQX is slightly less linear for the 5.5V case.

7.4.1.4 Other Vendor I Parameters

Six other parameters were tested over the specified range of temperature and VCC. These six parameters are Chip Deselect Time (TEHQZ), Write Pulse Width (TWLWH), Chip Select Setup Time (TELWH), Data Setup Time (TDVWH), Address Hold Time (TWHAX), and Data Hold Time (TWHDX). All measured values of these parameters for the 23 tested devices were found to be within the vendor's specified limits.

7.4.2 Vendor J AC Parameters

The AC characterization also measured TAVQV, TELQV, TAVWL and TAXQX for Vendor J. There were no recorded failures for this vendor at the two VCC levels (4.5V, 5.5V).

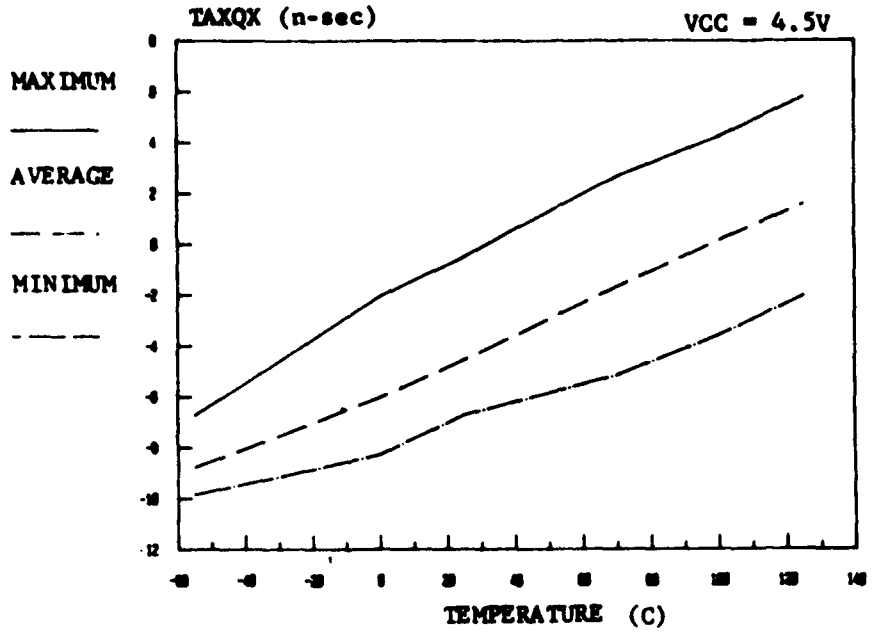
7.4.2.1 Address and Chip Enable Access Time

Address Access Time (TAVQV) is shown in Figure 7.12. TAVQV at VCC = 4.5V is an average of 3nS higher than at 5.5V. Access time at 5.5V displays some low temperature sensitivity which can be seen in the maximum value plot. All measurements of TAVQV were within Vendor J's specified limits.

Chip Enable Access times (TELQV), plotted in Figure 7.13, were similar at both levels of VCC. Chip Enable Access time is an average of 3 to 4nS higher for VCC = 4.5V. All devices characterized were within the specified limits for TELQV at the six temperatures and two levels of VCC.

7.4.2.2 Address Setup Time

Figure 7.14 shows a (min, avg, max) plot of Address Setup Time (TAVWL) for VCC = 4.5V and 5.5V and the six temperatures. TAVWL decreases with an increase of temperature for both levels of VCC. At 5.5V, TAVWL is an average of 3.5nS greater than at 4.5V. The plot at 5.5V also displays the same basic trend for the minimum and maximum curves. All measurements of TAVWL at both VCCs were within Vendor J's specified limits.



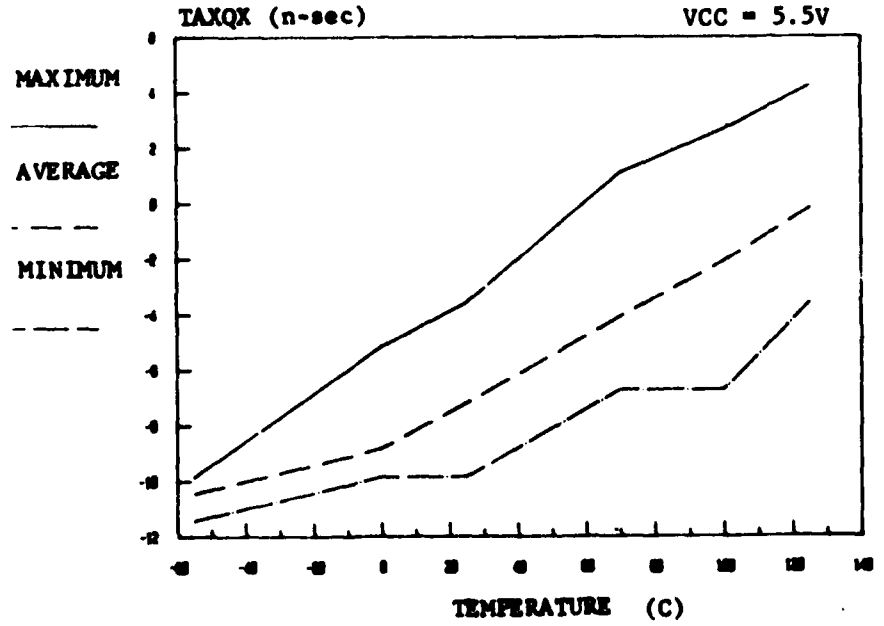
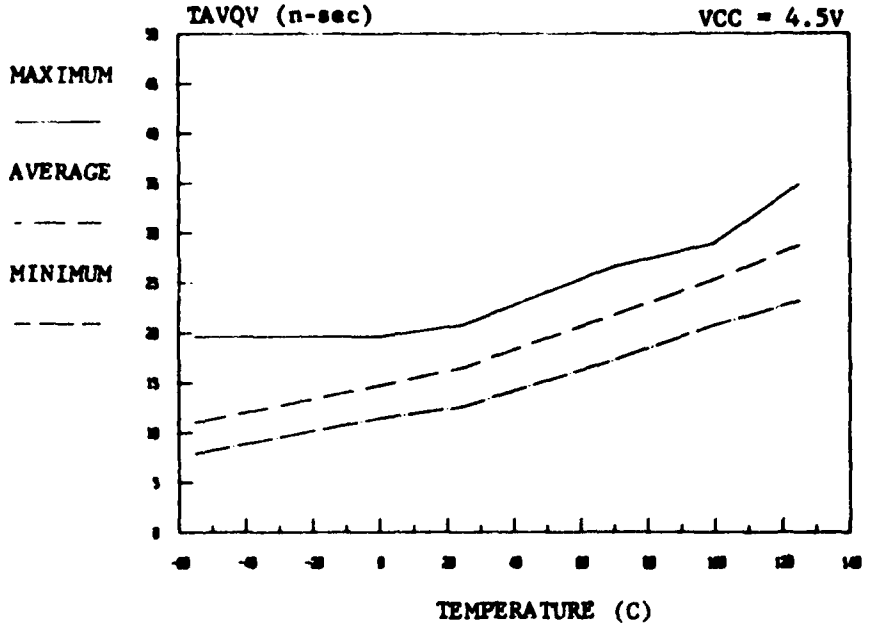


Figure 7.11 Vendor I - Address to Invalid Data Output Time vs. Temperature



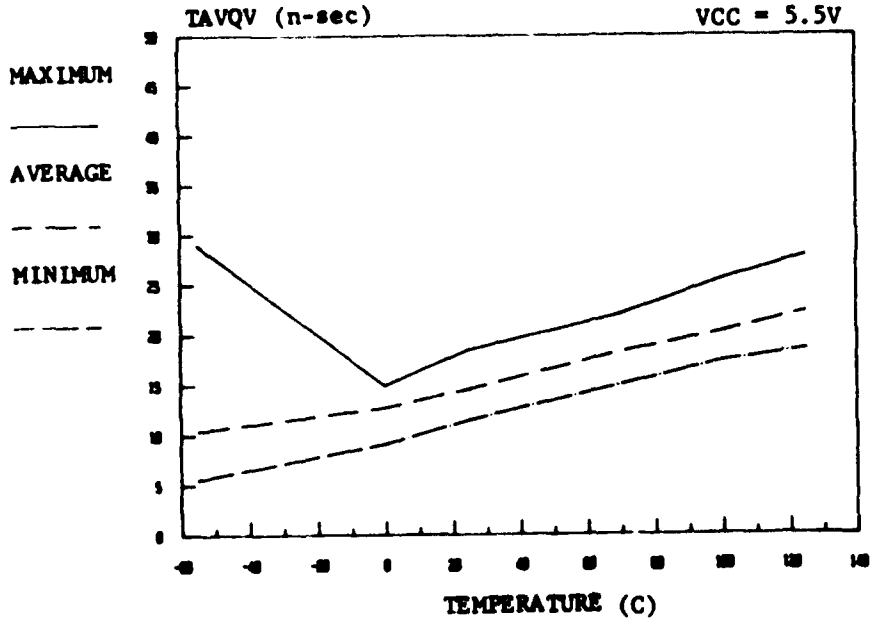
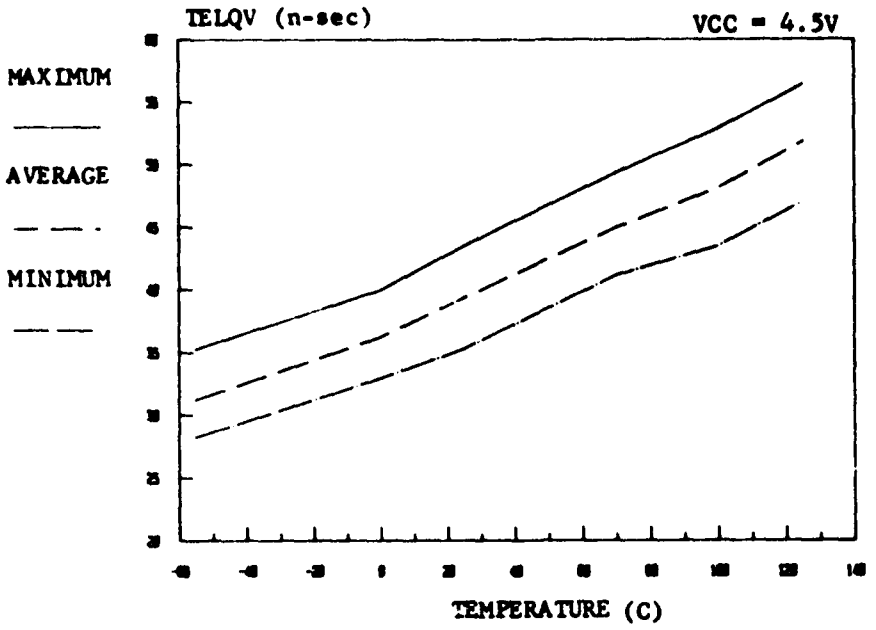


Figure 7.12 Vendor J - Address Access Time vs. Temperature



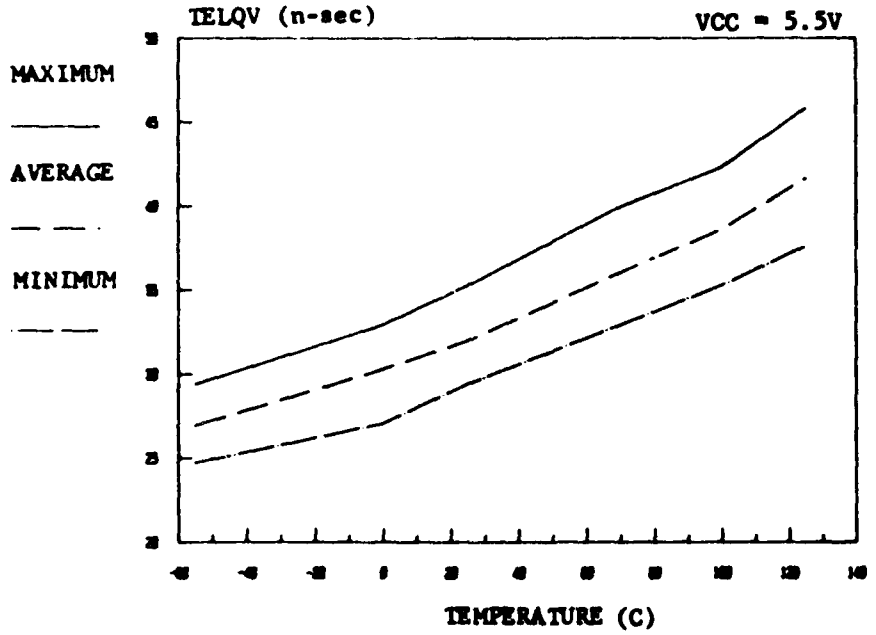
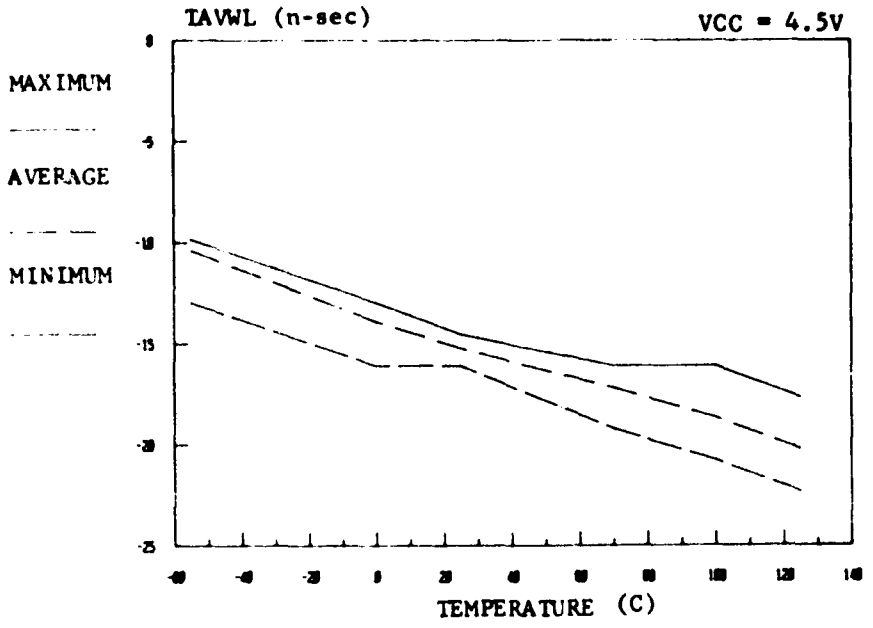


Figure 7.13 Vendor J - Chip Enable Access Time vs. Temperature



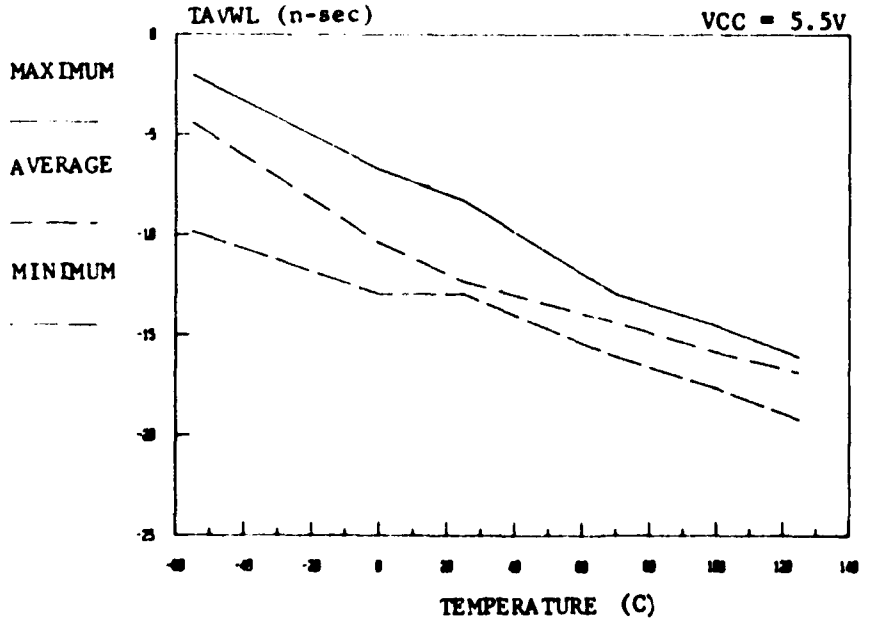


Figure 7.14 Vendor J - Address Setup Time vs. Temperature

7.4.2.3 Address to Invalid Output

The Address to Invalid Output parameter (TAXQX) for the Vendor J device is plotted in Figure 7.15. Both plots display an increase in TAXQX with increasing temperature. TAXQX for VCC = 4.5V is an average of 3 to 4nS higher than at 5.5V. There were no recorded failures of TAXQX at the six specified temperatures and two VCC levels.

7.4.2.4 Other Vendor J Parameters

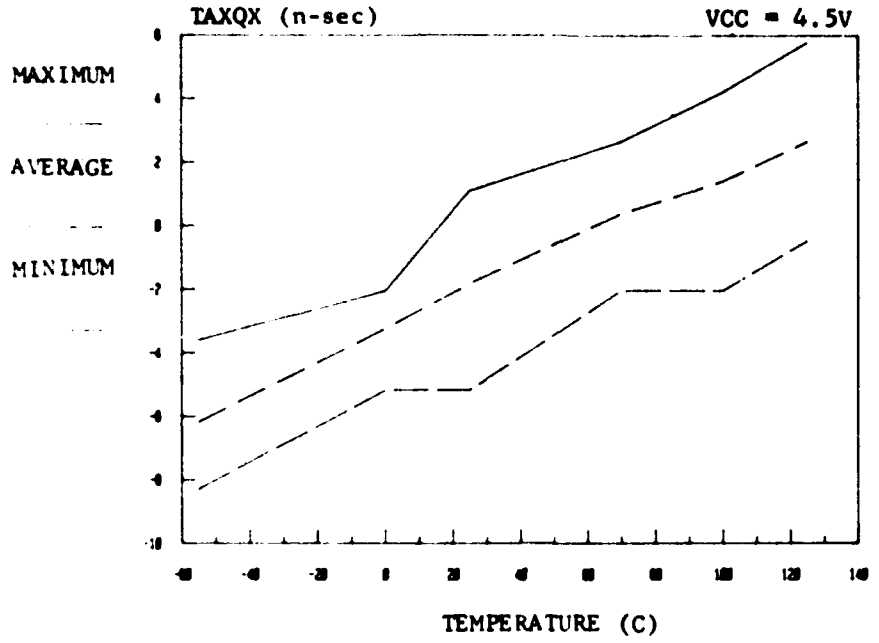
The other parameters tested for Vendor J at the six temperatures and two levels of VCC were TEHQZ, TWLWH, TELWH, TDVWH, TWHAX, and TWHDX. All measured values of these parameters were found to be within the specifications for Vendor J.

7.4.3 Vendor I, Vendor J Output Disable Time

A bench test was used to measure when the output reached a high impedance state. Output Disable Time was measured as output current decreased to zero. Table 7.7 lists data for both vendors. Ten devices from each vendor were tested in the VOH and VOL logic states. Vendor J is an average of 4 ns faster than Vendor I when the output turns off from either logic state (VOH or VOL). Output disable time is an average of 2 ns faster when turning off from the VOH logic state than the VOL state.

Table 7.7a Output Disable Time - Output initially at VOH

	Vendor I			Vendor J	
S/N	TOHQZ	Unit	S/N	TOHQZ	Unit
4	13	nsec	1	10	nsec
5	13		2	11	
7	14		3	10	
10	14		4	9	
11	15		5	10	
12	13		6	9	
15	13		7	12	
17	15		8	10	
19	13		10	10	
20	14		11	10	



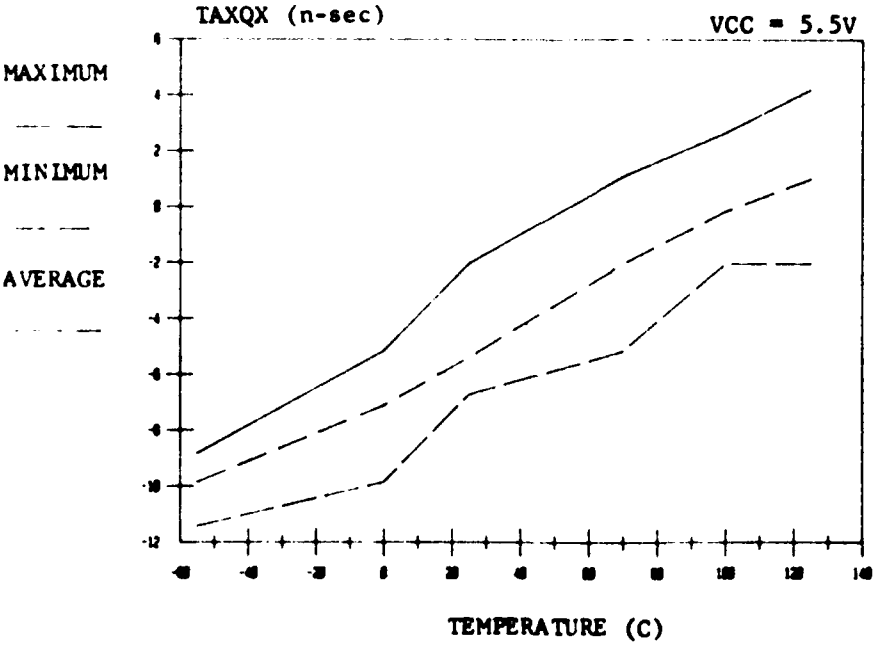


Figure 7.15 Vendor J - Address to Invalid Data Output Time vs. Temperature

Table 7.7b Output Disable Time - Output initially at VOL

S/N	Vendor I TOHQZ	Unit	S/N	Vendor J TOHQZ	Unit
4	14	nsec	1	12	nsec
5	15		2	13	
7	16		3	12	
10	15		4	12	
11	17		5	12	
12	16		6	11	
15	16		7	13	
17	19		8	12	
19	15		10	12	
20	16		11	12	

7.4.4. AC Characterization Summary

For all access and setup times, Vendor I was slightly slower than Vendor J. Vendor I also exhibited some sensitivity to the temperature extremes.

Output disable time was also slightly higher for Vendor I, than for Vendor J.

7.5 Pattern Sensitivity

Twenty devices from each vendor were subjected to March, Gallop, and Address Complement test patterns to determine their access time sensitivity at 25°C and VCC = 5V. Data was taken at logic levels of VIH = 2.0V, VIL = 0.8V and VIH = 3.0V, VIL = 0.4V. Table 7.8 lists average worst case access times for the three test patterns at each set of logic levels. Overall, the access time sensitivity to the March, Gallop, and Address Complement test patterns for both vendors is minimal.

Both the March and the Address Complement patterns yield access times similar to the Gallop but require significantly less execution time. Therefore, either the March or Address Complement test is preferred for the slash sheet. The Address Complement pattern exercised the address decode circuitry more dynamically than the March because of its complementing action each memory cycle. It is expected that this will be more effective than the March in detecting decoder response problems. (The Gallop pattern has long been considered one of the most effective address decoder tests but its long execution time is a significant disadvantage.)

Table 7.8 Test Pattern vs. Worst Case Access Time(TAVQV) at 25°C and VCC = 5V

CASE 1: VIH = 2.0V, VIL = 0.8V

	MARCH	GALLOP	ADDRESS COMPLEMENT
Vendor I (avg. of 20 devices)	24.5ns	24.5ns	24.5ns
Vendor J (avg. of 20 devices)	16.4ns	17.5ns	16.5ns

CASE 2: VIH = 3.0V, VIL = 0.4V

	MARCH	GALLOP	ADDRESS COMPLEMENT
Vendor I (avg. of 20 devices)	24.3ns	24.2ns	24.5ns
Vendor J (avg. of 20 devices)	14.7ns	13.0ns	13.0ns

7.6 Power-On Readiness

Power-on readiness testing was performed only on Vendor I devices since only they employed a substrate bias generator. This test consisted of two portions performed at 25°C:

1.) bench measurement of the substrate voltage stabilization time.
2.) automatic measurement of the delay time between power-on and reliable device operation.

The stabilization measurement was the time needed for the substrate bias to reach the -3V nominal value. This measurement was performed on only three devices since these had an external substrate contact. All three exhibited a 70 usec stabilization time.

Power-on readiness data displayed in Figure 7.16 was taken on five devices at various temperatures. Four out of five devices exhibited similar but non-linear behavior. A trend is established between 25°C and 110°C. But, for the four devices, this trend does not apply at low temperatures. A single device, #13, exhibited the same trend at all temperatures.

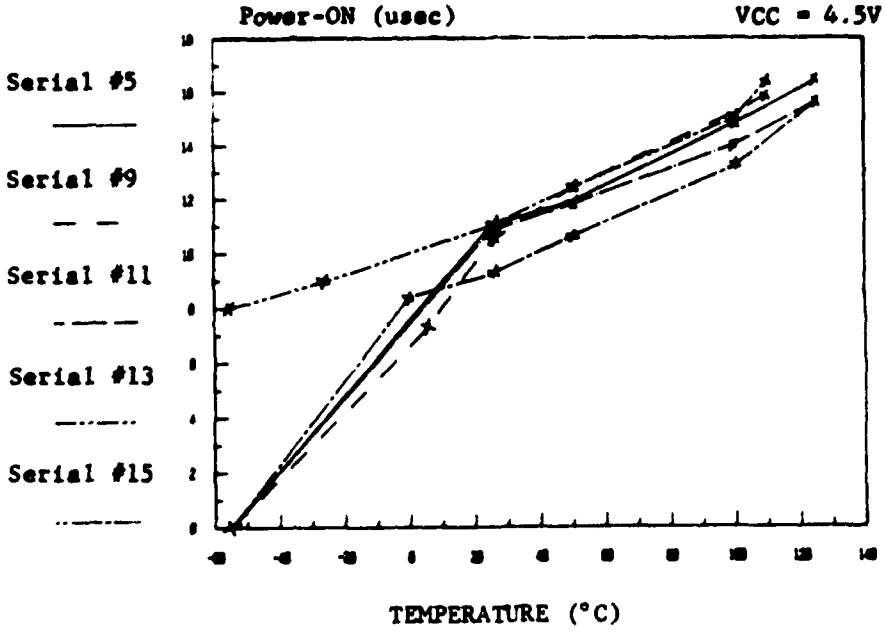


Figure 7.16 Vendor I Power-ON Readiness Time vs. Temperature for 5 Devices

7.7 Introduction (2K X 8 Static RAMS)

Three separate 2K X 8 devices, the Mostek 4802P, the Harris MI-6516, and the IDT 6116LP, were originally characterized on this contract. The Mostek 4802P has since been discontinued, therefore the focus of this discussion is on the IDT and Harris devices only.

The IDT 6116P and the Harris MI-6516 are both 16K CMOS Static Rams organized as 2K X 8. The Harris device is constructed utilizing an all CMOS process, whereas, IDT is a mixed MOS process employing an N-MOS memory array surrounded by a CMOS periphery. Both devices feature individual chip enable and output enable functions. These functions, along with the byte wide configuration, make them ideally suited to microprocessor based systems. The 6516 is a synchronous device, i.e. the address inputs are 'latched' by the falling edge of the chip enable pulse. Because of this, the 6516 has no address access time as such, but instead has an access time which is the sum of the address set-up time and the chip enable access time. The vendor designations for each device will be as follows:

Harris	MI-6516	Vendor D
IDT	6116LP	Vendor J

Table 7.9 summarizes the device part number, date codes, specified access times, and lot quantities.

Table 7.9 Devices Procured For Characterization

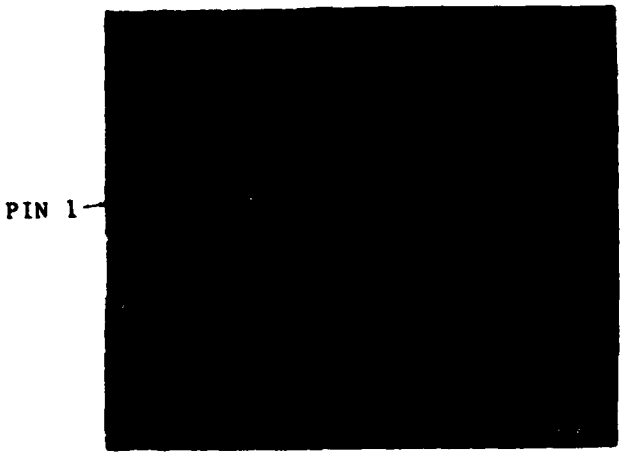
Vendor	Part No.	Access Time	Date Code	Quantity
D	MI-6516-8	250	8145	25
J	6116L	150	8249	24

Photos of the dies from each vendor are shown in Figure 7.17, while Table 7.10 below gives the chip dimensions.

The devices were packaged in 24 pin ceramic dual-in-line dips whose pin configurations are shown in Figure 7.18. Although the Harris device is synchronous, both vendors were pin for pin compatible.

Table 7.10 2K X 8 Static Ram Chip Dimensions

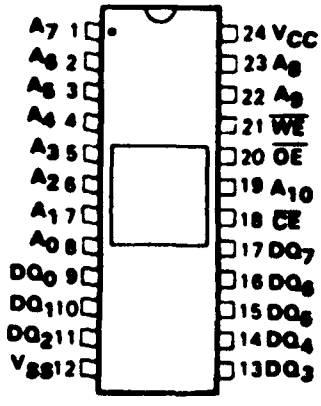
Vendor	Length (mm)	Width (mm)	Area (sq. mm)
D	5.94	5.11	30.35
J	5.16	4.06	20.95



VENDOR D

VENDOR J

FIGURE 7.17 DIE PHOTOS - 2K X8 STATIC RAMS (12.3X)



Vendor D, Vendor J

Figure 7.18 2Kx8 Pin Configuration

7.8 Incoming Test

All devices from each vendor passed the incoming test.

7.9 DC Parameters

The DC parameters and test conditions specified by the two manufacturers are listed in Table 7.11. All parameters were tested at -55°C, 0°C, 25°C, 70°C, 100°C, and 125°C.

Table 7.11 Vendor Specified DC Parameters

		Vendor D		Vendor J	
Symbol	Parameter	Min	Max	Min	Max
IIH,IIL	Input Leakage Current	-1.0	+1.0uA	-	2.0uA
VOL	Output Voltage Low	-	0.45V	-	0.4V
VOH	Output Voltage High	2.4V	-	2.4V	-
ICC1	Supply Current (Active)	-	20mA	-	60mA
ICC2	Supply Current (Standby)	-	100uA	-	12mA

7.9.1 Leakage Current (IIH,IIL)

The leakage currents for Vendors D and J were typical of similar CMOS devices and were all well within +/- 1.0uA. Since the magnitudes of these currents approach the measurement capabilities of the S-3270 test system, general trends could not be discerned and therefore will not be discussed.

7.9.2 Output Voltage High (VOH)

For VOH, both the magnitudes and the general trends are different. Vendor D exhibits a decreasing VOH measurement as temperature increases while Vendor J's output voltage high increases with temperature (see Figures 7.19a and 7.20a). Worst case magnitudes for Vendor D are 4.44 volts at -55°C to 4.34 volts at 125°C. For Vendor J, 3.52 volts at -55°C and 3.84 volts at +125°C are the worst case magnitudes. All values were well above the 2.4 volt minimum VOH as specified by the vendors.

7.9.3 Output Voltage Low (VOL)

The magnitudes and general trends for both vendors were very similar for VOL. Both exhibited increasing VOL for increasing temperature with worst case magnitudes of 90mV at -55°C to 275mV at +125°C(see Figures 7.19b and 7.20b). Although Vendor J yielded a significantly tighter spread between maximum and minimum values all values were well below the vendor specified VOL maximum of 450mV.

7.9.4 Active Supply Current (ICC1 and ICC2)

The active supply currents were measured with the device in a constant read cycle (ICC1) and in a constant write cycle (ICC2). For Vendor J the difference between ICC1 and ICC2 was insignificant; i.e. the active supply current was not affected by the type of cycle or operation being performed. These values were found to be decreasing for increasing temperature, with worst case magnitudes being 57.5mA at -55°C to 27.5mA at +125°C, below the 60mA maximum specified by the vendor. The active supply current for Vendor D was approximately 4mA higher for a write operation than for a read operation(see Figure 7.21a, b, and c). This sensitivity may be ignored when considering the fact that it is less than 5% of the maximum specified limit. Worst case magnitudes for Vendor D were 10mA at -55°C and 11mA at +125°C, again, well within the specified limits.

7.9.5 Input/Output Pin Capacitance

Table 7.12a Vendor D Min, Avg, and Max Pin Capacitance

Pin	Min	Avg	Max	Limit
A0-A10	2.0	2.45	4.1	8pf
E,W,G	2.55	3.8	4.7	8pf
DQ0-DQ7	4.15	5.2	6.15	10pf

Table 7.12b Vendor J Min. Avg. and Max Pin Capacitance

Pin	Min	Avg	Max	Limit
A0-A10	3.4	4.1	5.9	6pf
E,W,G	3.7	4.2	4.9	6pf
DQ0-DQ7	5.1	5.6	6.2	8pf

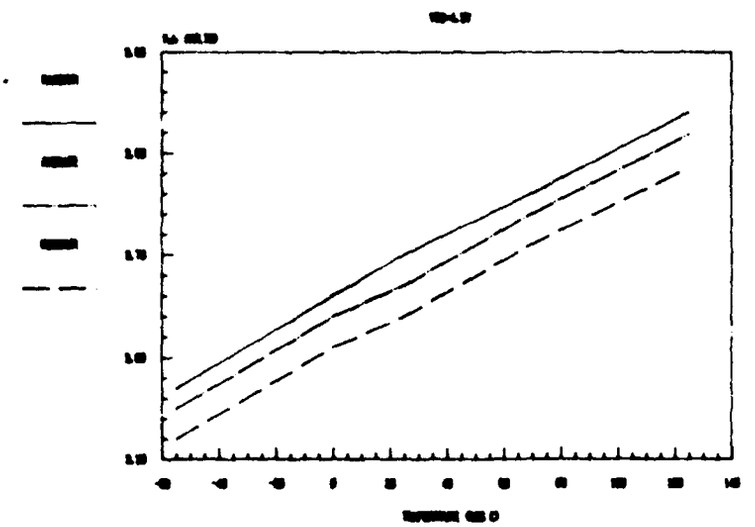


Figure 7.19a Vendor J - Output High Voltage (VOH)

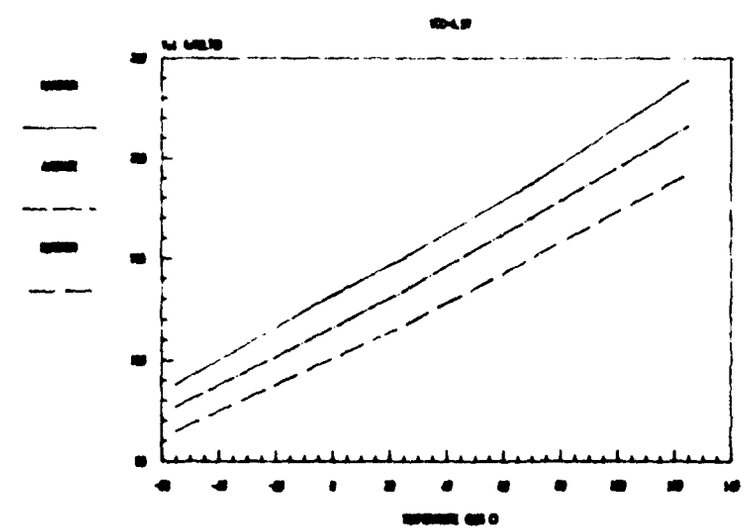


Figure 7.19b Vendor J - Output Low Voltage (VOL)

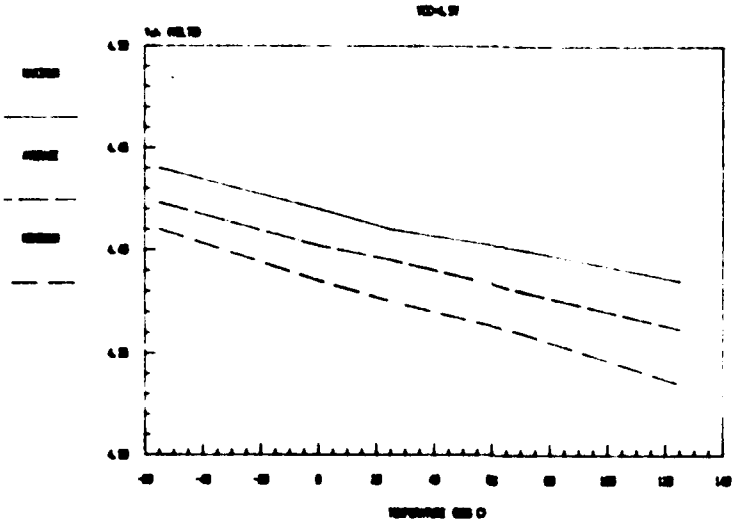


Figure 7.20a Vendor D - Output High Voltage (VOH)

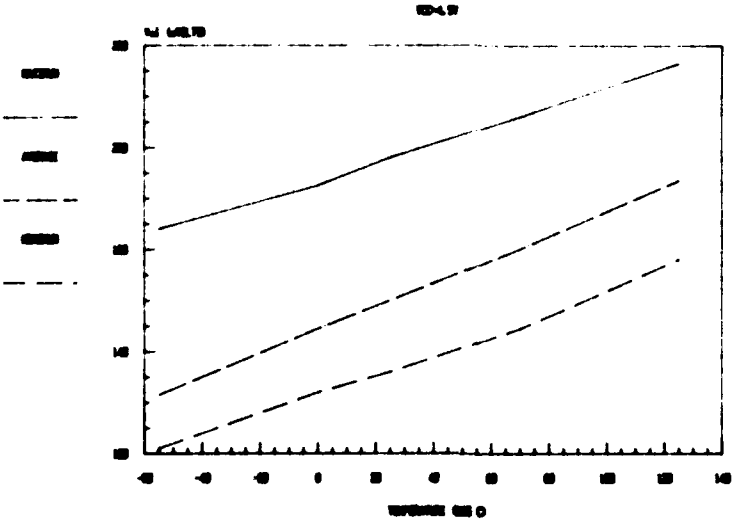


Figure 7.20b Vendor D - Output Low Voltage (VOL)

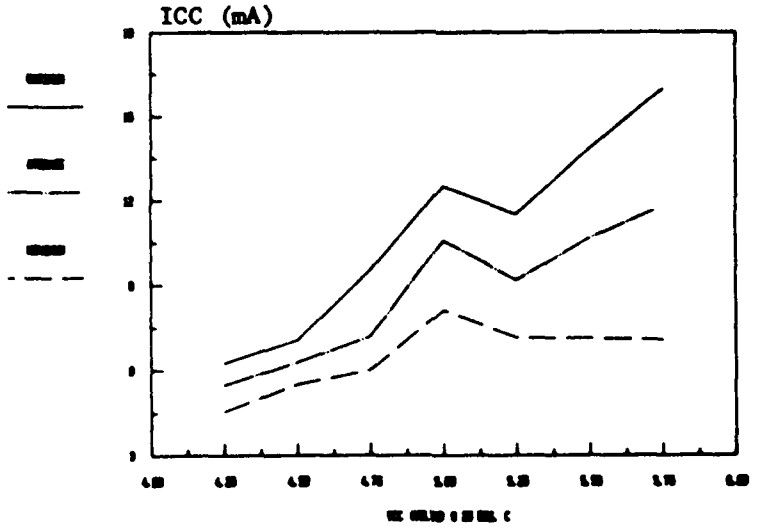


Figure 7.21a Vendor D - Supply Current vs. VCC (Temp. = 25°C)

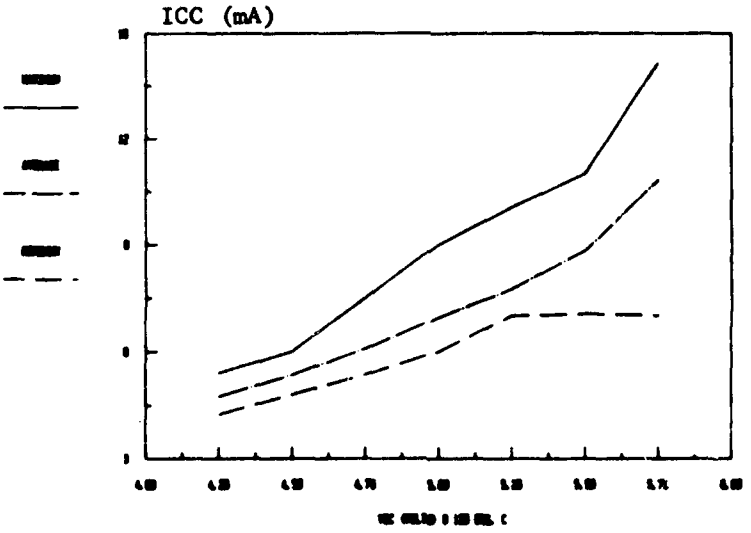


Figure 7.21b Vendor D - Supply Current vs. VCC (Temp. = 125°C)

AD A147 657 ELECTRICAL CHARACTERIZATION OF VLSI (VERY LARGE SCALE INTEGRATION) MEMORIES(U) GENERAL ELECTRIC CO PITTSFIELD MA ORDNANCE SYSTEMS J SCHWEHR ET AL. MAY 84 3/3

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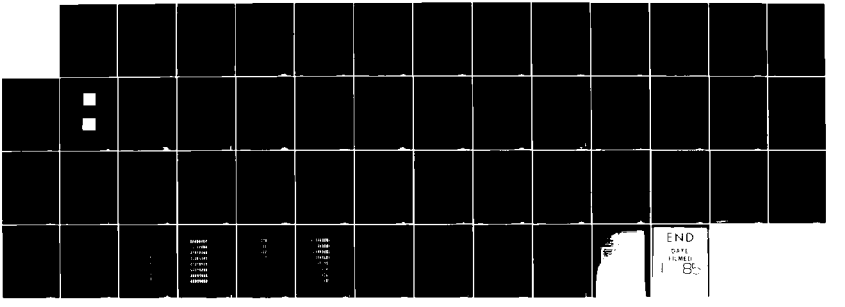

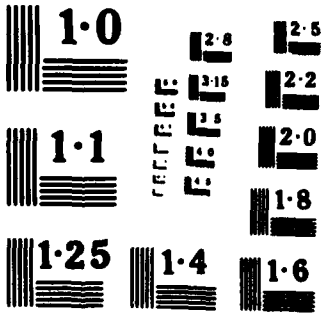
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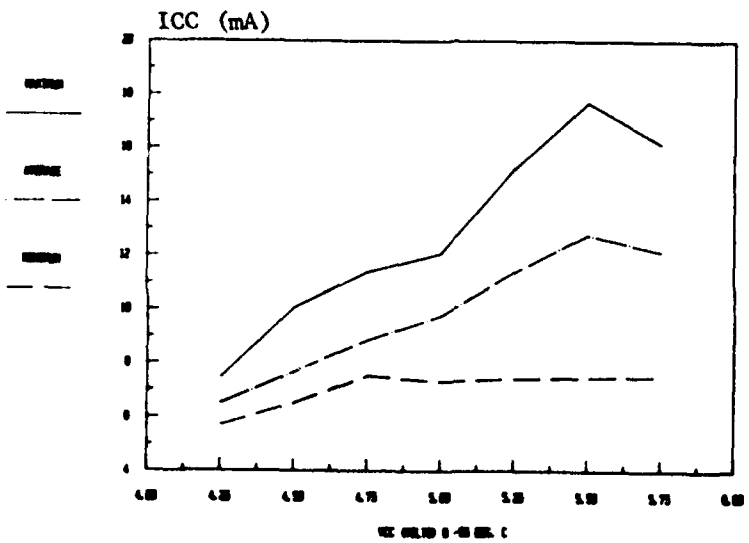


Figure 7.21c Vendor D - Supply Current vs. VCC (Temp. = -55°C)

7.10 AC Characterization

The AC parameters and their vendor specified limits are listed in Table 7.13. Refer to Appendix B for abbreviations and waveform symbols used in this section.

Table 7.13 Vendor Limits for AC Parameters

	Vendor D		Vendor J		
	Min	Max	Min	Max	Unit
TAVQV	---	---*	---	150	nsec
TELQV	---	250	---	150	
TAVEL	10	---	20	---	
TOHQZ	---	100	---	50	

* Not applicable to vendor D

7.10.1 Address Access Time (TAVQV)

This parameter applies to Vendor J only. TAVQV was measured while employing a march pattern (see Appendix C) with VCC at 4.5 volts and again at VCC at 5.5 volts. The average address access time at 4.5 volts increased from 80 nsec at -55°C to 92 nsec at +125°C in a relatively linear fashion(see Figures 7.22a and 7.22b). Worst case measurements were 102 nsec maximum at 70°C and 72 nsec minimum at -55°C. With a VCC of + 5.5 volts, the average access times were 118 nsec at -55°C, decreasing to 82 nsec at 0°C. From 0°C to +125°C the curve remained relatively flat.

7.10.2 Chip Enable Access Time (TELQV)

For Vendor J, the trends for chip enable access times at 4.5 volts VCC and 5.5 volts VCC are very similar to those for address access times. The magnitudes were less with the average TELQV at 4.5 volts VCC increasing from 62 nsec at -55°C to 83 nsec at +125°C in a linear fashion. As with the TAVQV, the average chip enable access time at 5.5 volts VCC decreased steeply from 74 nsec at -55°C to 55 nsec at 0°C and (refer to Figures 7.23a and 7.23b) then increased slightly to 62 nsec at +125°C. Minimum values ranged from 44 nsec at -55°C to 60 nsec at +125°C. Vendor D exhibited similar behavior with chip enable access times at VCC=4.5 volts increasing from 65 nsec at -55°C to 115 nsec at +125°C(see Figures 7.24a, b, and c).

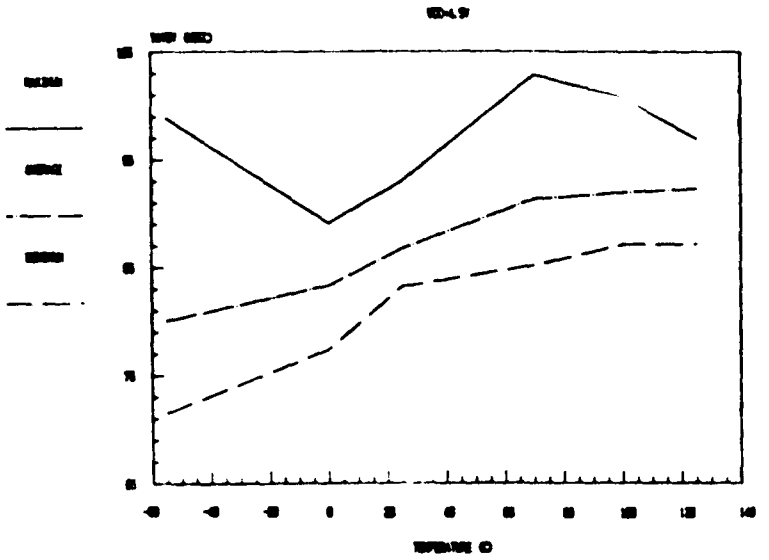


Figure 7.22a Vendor J - Address Access Time (VCC=4.5V)

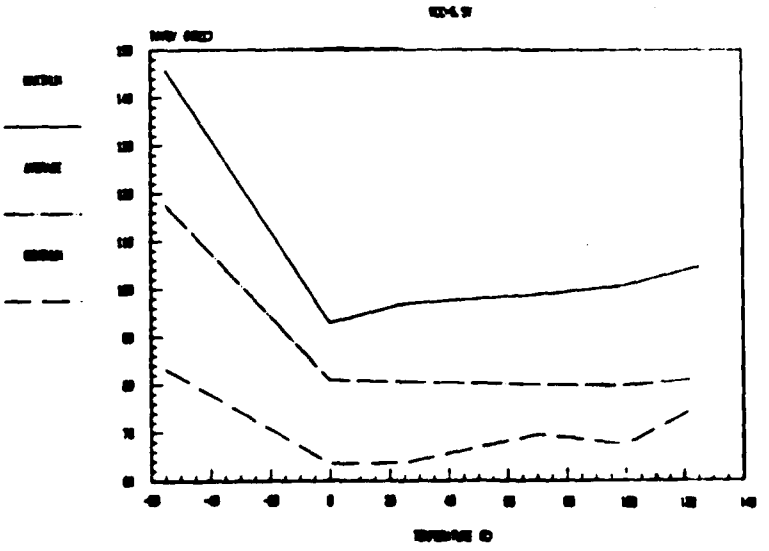


Figure 7.22b Vendor J - Address Access Time (VCC=5.5V)

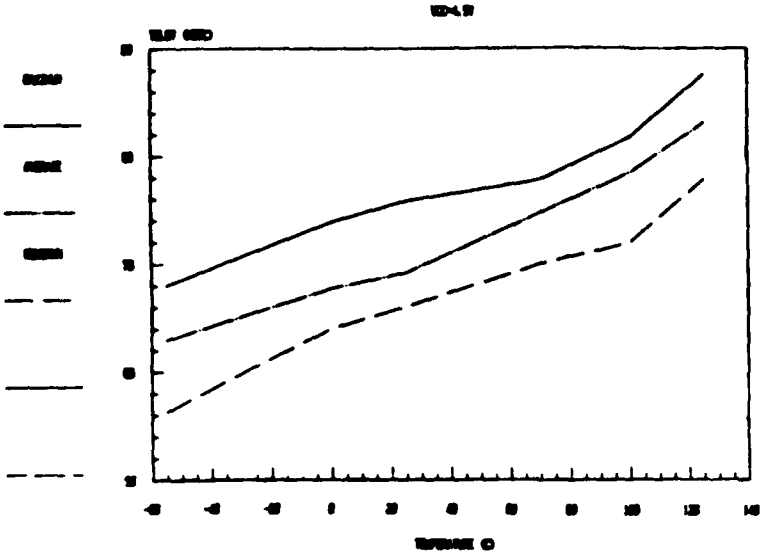


Figure 7.23a Vendor J - Chip Enable Access Time (VCC=4.5V)

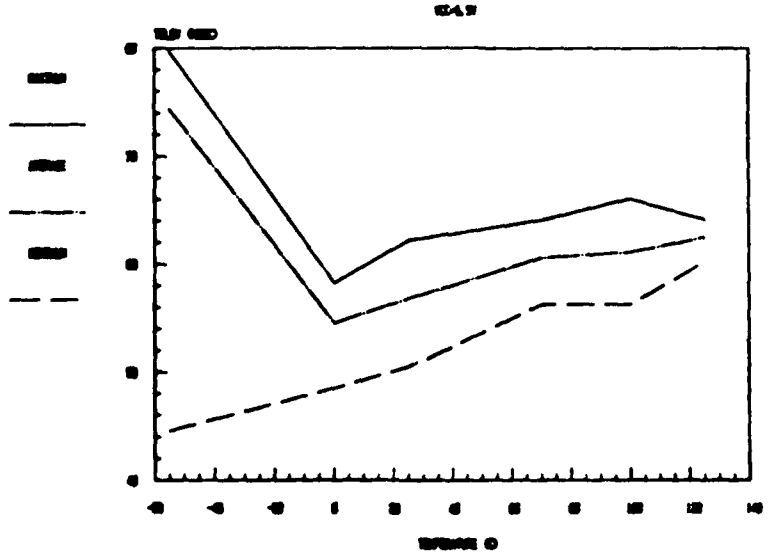


Figure 7.23b Vendor J - Chip Enable Access Time (VCC=5.5V)

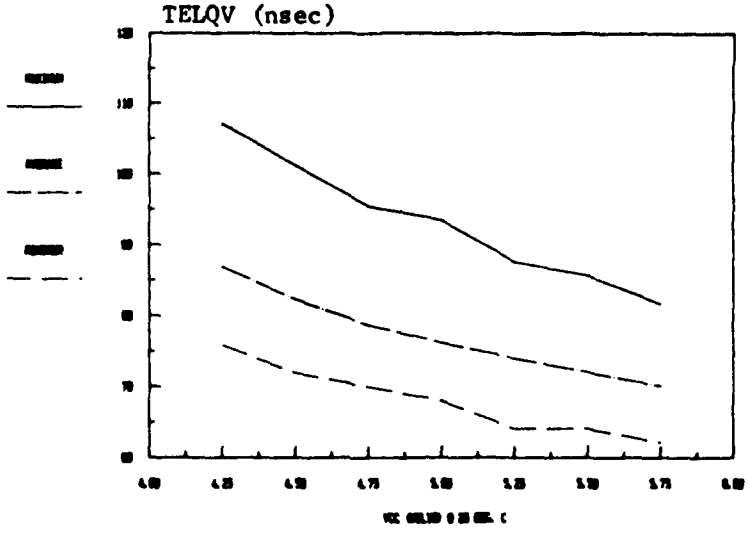


Figure 7.24a Vendor D - Chip Enable Access Time vs. VCC (Temp. = 25°C)

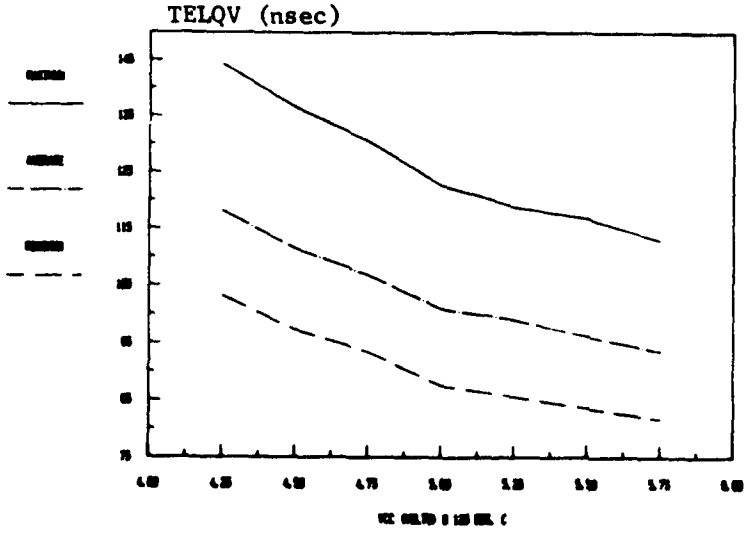


Figure 7.24b Vendor D - Chip Enable Access Time vs. VCC (Temp. = 125°C)

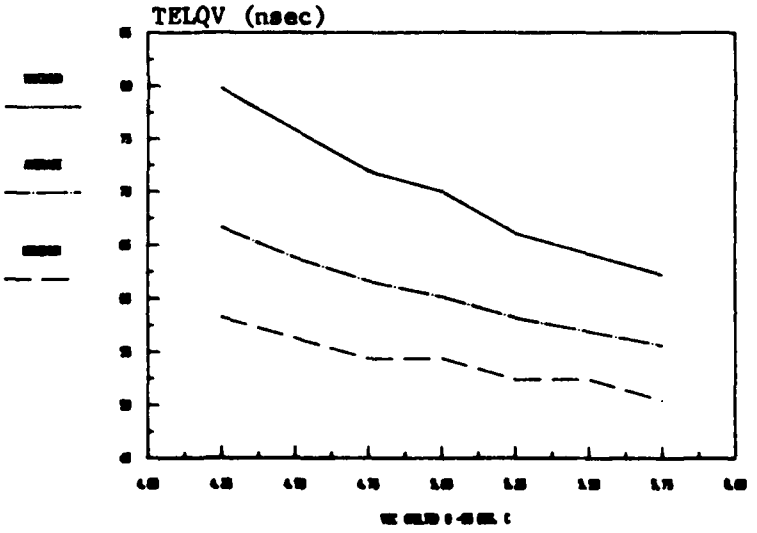


Figure 7.24c Vendor D - Chip Enable Access Time vs. VCC (Temp. = -55°C)

7.10.3 Address Setup Time (TAVEL)

Vendor D devices exhibited a slight sensitivity to both temperature and VCC(see Figures 7.25a, b, and c). The general trends were for decreasing setup time with increasing VCC and increasing setup time with increasing temperature. At a VCC of 4.5 volts , setup times increased from 8 nsec at -55°C to 14 nsec at +125°C and at a VCC of 5.5 volts, TAVEL increased from 7 nsec at -55°C to 12.5 nsec at +125°C (average values). Although these values exceed the vendor's minimum specification of 10 nsec, it is important to note that the only specification sheets available at the time of this writing were a product preview sheet and an advance information sheet. The data indicates that the Vendor J specification of 20 nsec appears to be more adequate than that of Vendor D. Vendor J devices displayed significantly different behavior than that of Vendor D with setup times decreasing with increasing temperature and very little sensitivity to VCC (less than 1 nsec between 4.5 and 5.5 volts VCC)(see Figures 7.26a and 7.26b). The average TAVEL values for Vendor J were 7.4 nsec at -55°C increasing linearly to 11.5 nsec at + 125 C at a VCC of 4.5V. For VCC = 5.5V TAVEL was found to be 6.8 nsec at -55 C increasing linearly to 10.5 nsec at +125°C. All values were well within the vendors specified minimum of 20 nsec.

7.10.4 Output Disable Time (TOHQZ)

Availability problems with Vendor D devices resulted in their being received very late in the contract. This precluded the bench testing of output buffer turn-off time and pattern sensitivity. Ten Vendor J devices were bench tested for TOHQZ. The data is presented in Table 7.14 below:

Table 7.14 Output Disable Time - Vendor J

S/N	From VOL	From VOH	unit
50	12	10	nsec
51	11	10	
52	10	9	
53	11	11	
54	12	11	
55	12	11	
56	12	11	
57	11	10	
58	12	12	
59	12	11	

All TOHQZ measurements were well below the manufacturers specified maximum limit of 50 nsec.

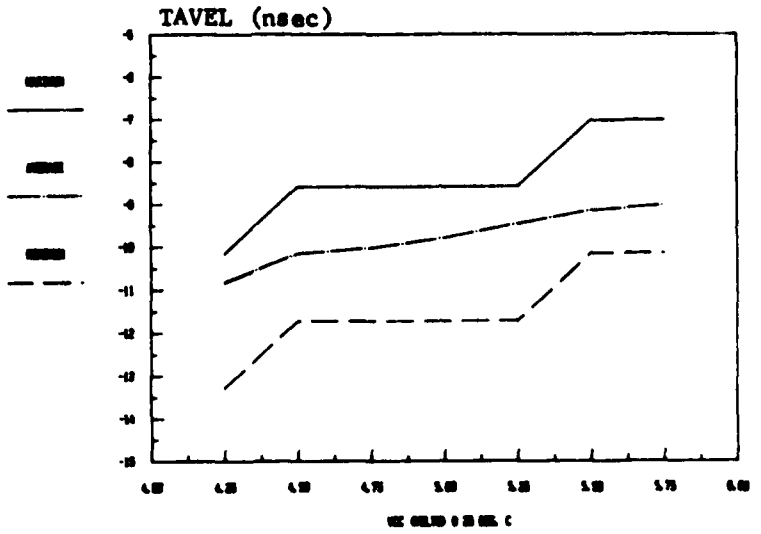


Figure 7.25a Vendor D - Address Setup Time vs. VCC (Temp. = 25°C)

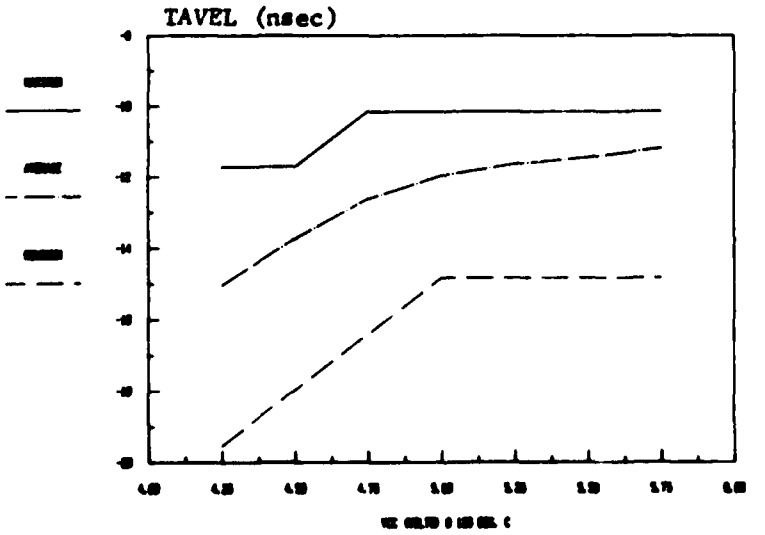


Figure 7.25b Vendor D - Address Setup Time vs. VCC (Temp. = 125°C)

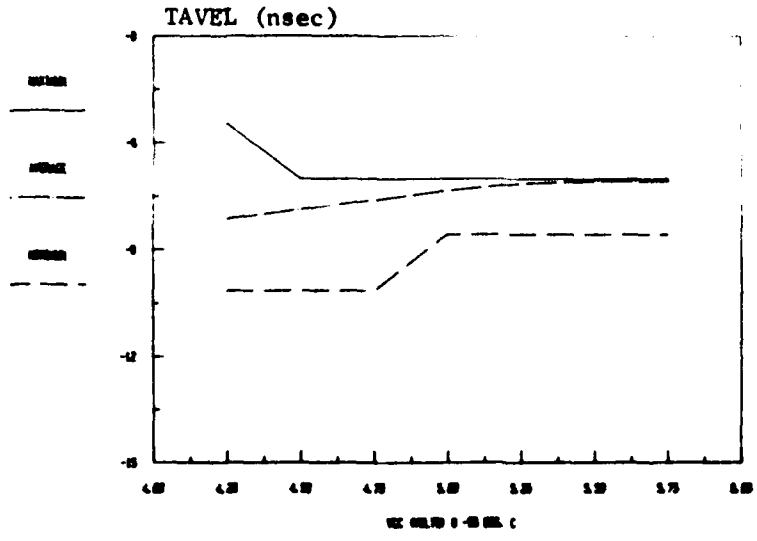


Figure 7.25c Vendor D - Address Setup Time vs. VCC (Temp. = -55°C)

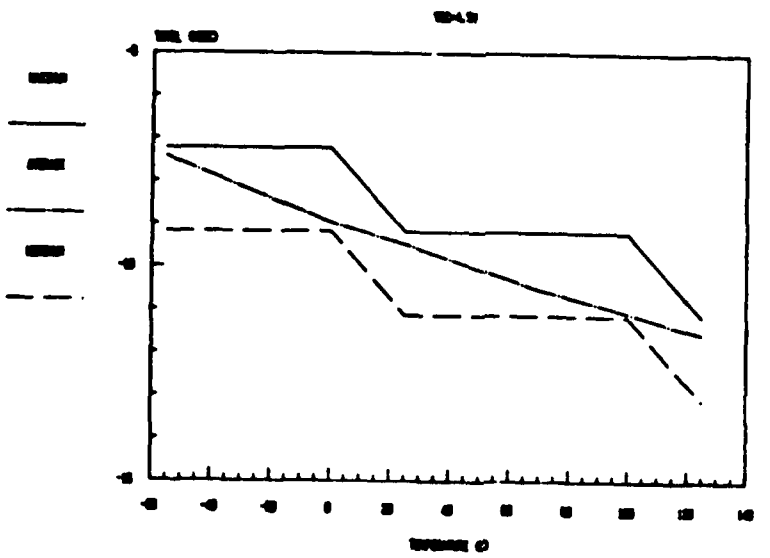


Figure 7.26a Vendor J - Address Setup Time (VCC=4.5V)

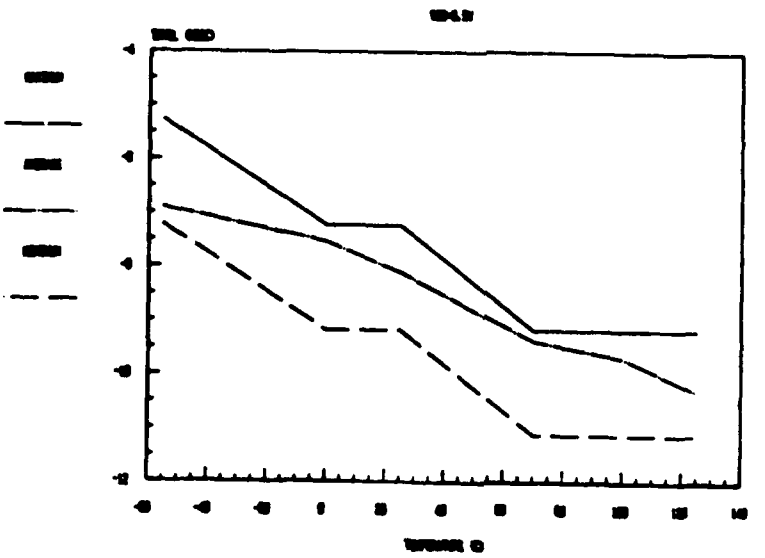


Figure 7.26b Vendor J - Address Setup Time (VCC=5.5V)

7.10.5 Comparison of Vendors' AC Characteristics

Despite Vendor D's 250 nsec maximum access time specification, their AC performance was remarkably similar to that of Vendor J devices. Address setup times (TAVEL) for both vendors were in the 5 to 20 nsec range. Average access time comparisons are shown in Table 7.15 below.

Table 7.15 Comparison of Average Access Times

		Vendor D	Vendor J
VCC=4.5V	-55°C	70 nsec	80 nsec
	25°C	92	86
	125°C	125	92
VCC=5.5V	-55°C	60 nsec	118 nsec
	25°C	81	80
	125°C	108	80

With the exception of two extremes, i.e. VCC=4.5V at +125°C and VCC=5.5V at -55°C, both Vendors are within 30 nsec of one another. This is significant in view of the fact that the difference in the specifications is 100 nsec. In both cases, the address access time and chip enable access time specifications are more than adequate. The synchronous mode of the Vendor D device is clearly a differentiating aspect.

7.11 Pattern Sensitivity

Pattern sensitivity testing was accomplished using various types of patterns and measuring the resulting address access times. Since the Vendor D devices are synchronous, address patterns impact the data access time very little, and thus sensitivity testing was not performed. Six Vendor J devices were tested for pattern sensitivity. Patterns and their corresponding address access times are shown in Table 7.16.

Table 7.16 Vendor J- Pattern Sensitivity for Six Devices

	Vendor J S/N						Units
Pattern	50	51	52	53	55	56	nsec
Galloping Address	61.7	53.9	59.8	65.6	59.8	59.8	
March	59.8	53.9	59.8	65.6	59.8	59.8	
Inter-Write Recovery	59.8	53.9	57.8	61.7	59.8	59.8	
Address Complement	59.8	53.9	59.8	65.6	59.8	59.8	
Galloping Row	57.9	53.9	55.9	61.7	57.8	59.8	
Galloping Column	57.9	52	55.9	59.8	57.8	57.8	
Inter-Write Recovery (Row)	59.8	52	55.9	59.8	57.8	57.8	
Inter-Write Recovery (Column)	57.9	52	55.9	61.7	57.8	57.8	

All measurements were made at 25°C. This data indicates that Vendor J devices are essentially not sensitive to the various pattern types. The worst case difference among the various patterns was 5.8 nsec with the average delta being 3.2 nsec.

8. PAL16R8

8.1 Introduction

The PAL16R8 is one of a number of array logic devices employing fusible link technology to implement relatively complex boolean functions. The device technology is bipolar and the circuit is arranged in a sum-of-products configuration to facilitate the programming of various logic functions. The PAL16R8 consists of 64 AND gates each with 32 programmable inputs. These AND gates are arranged in groups of eight with the output of each feeding a fixed OR gate. The output of the OR gate is latched and fed back to the inputs thereby facilitating not only combinatorial functions but sequential functions as well.

Sources for the devices were Monolithic Memories Incorporated (MMI) and National Semiconductor (2nd source for MMI). These two manufacturers will hencetorth be referred to as Vendor F and Vendor B respectively. Die photos are shown in Figure 8.1 and the pin configuration for the device is shown in Figure 8.2. Device quantities received, as well as part numbers and date codes are shown in Table 8.1 below and chip dimensions are displayed in Table 8.2.

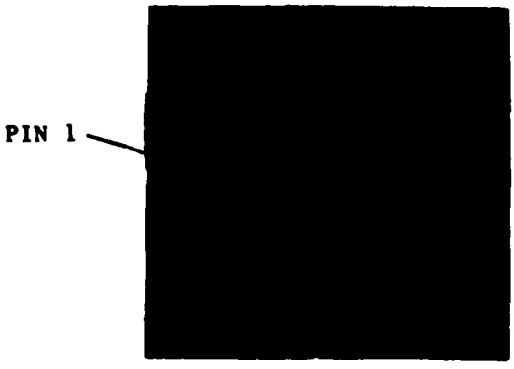
Table 8.1 Devices Provided for Characterization

Vendor	Part No.	Date Code	Quantity
F	16R8MJ	8201	20
F	16R8MJ	8125	10
B	16R8CJ	8216	10
B	16R8CJ	8219	10

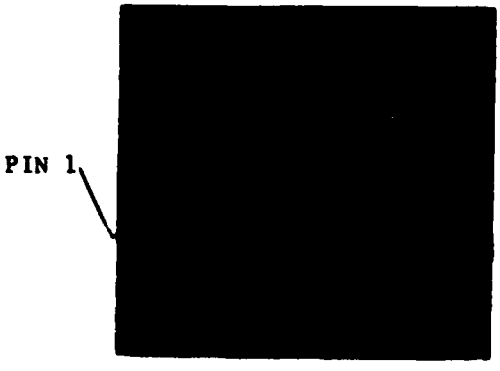
Table 8.2 16R8 PAL Chip Dimensions

Vendor	Length (mm)	Width (mm)	Area (sq. mm)
F	3.58	3.38	12.10
B	3.51	3.38	11.86

Programming of the devices was accomplished on a Data I/O system 19 PROM Programmer and the Tektronix S-3270 test system. Programming capability on the S-3270 was developed primarily to characterize the device programming parameters. Four separate fuse patterns were developed such that all internal nodes could be excercised and all fusible links within the device could be collectively programmed. These patterns are illustrated in Appendix B.

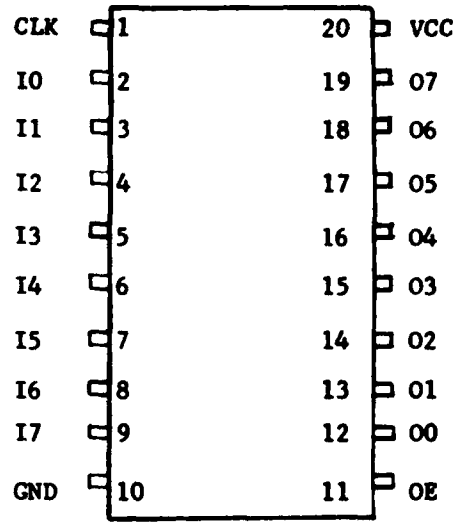


VENDOR B



VENDOR F

FIGURE 8.1 DIE PHOTOS - 16K X8 PAL (14.84X)



Vendor B, Vendor F

Figure 8.2 16R8 PAL Pin Configuration

8.2 Incoming Test

All devices passed the incoming test.

8.3 DC Parameters

The PAL16R8s exhibited DC behavior typical of bipolar devices. The parameters characterized include supply currents, input clamp diode measurements, output voltage high and low measurements, output short circuit current, and input voltage threshold measurements. Test data was obtained using standard test techniques on an automatic tester.

The DC characterization of the PAL16R8 was accomplished utilizing the following DC parameters and conditions as shown in Table 8.3.

Table 8.3 Vendor Specified Limits for DC Parameters

		VENDOR B		VENDOR F		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	4.5	5.5	Volt
ICCH	Supply current (VCC=5.5V)		180		225	mA
ICCL	Supply current (VCC=4.5V)					
IIL	Input current low		-0.25		-0.25	mA
IIH	Input current high		25		25	uA
VIC	Input clamp diode voltage		-1.5		-1.5	Volt
VOL	Output voltage low		0.5		0.5	Volt
VOH	Output voltage high	2.4		2.4		Volt
IOS	Output short circuit current	-30	-130	-30	-130	mA
VTH	Input threshold voltage	0.8	2.0	0.8	2.0	Volt

Following is a summary and analysis of the data obtained during characterization of these PAL devices.

8.3.1 Input Leakage Current (IIL,IIH)

Input leakage currents IIH and IIL were measured by forcing worst case conditions of 2.4V VIH and 0.4V VIL at VCC = 5.5V on each input. All leakage currents were well within the specifications set forth by the vendors over the full temperature range(See Figures 8.3 and 8.4).

8.3.2 Logic Output Voltage (VOH,VOL)

The output voltage measurements were accomplished by first applying the proper stimulus to achieve the desired output state, low or high. Secondly, the output was forced with the appropriate current, IOL = 12mA and IOH = -2.0mA for VOL and VOH respectively and the resulting voltage measured. VCC was set to the minimum of 4.5V and the input logic levels were 0.8V and 2.0V for VIL and VIH respectively. The spread between maximum and minimum VOL measurement was approximately 100mV with the average VOL being 300mV at -55°C and decreasing at a fairly linear rate to 250mV at 125°C(See Figures 8.5 and 8.6). VOH, on the other hand, was increasing with temperature with the average 2.8V at -55°C rising to 3.4V at 125°C. All values exceeded the specified minimum at 2.4V over the full MIL temp range.

8.3.3 Input Voltage Threshold (VTH)

Threshold voltage was obtained by incrementing or decrementing the input logic levels in 10mV increments until the appropriate change occurred at the outputs. This process was repeated on each pin to obtain individual threshold voltages. To account for hysteresis, an average of two threshold measurements, one obtained by incrementing from VIL and the other by decrementing from VIH, was taken as the threshold value. The general trend for VTH was to decrease linearly with increasing temperature(Figures 8.7 and 8.8). Typical values ranged from 1.66 volts at -55°C to 1.2 volts at +125°C. The nominal value at +25°C was approximately 1.52 volts which is well within and close to the center of the maximum VIL specification of 0.8V and the minimum VOH specification of 2.0V. Although no vendor specification, as such, exists for VTH, the parameter was predictable and well behaved as expected.

8.3.4 Supply Current (ICC)

Supply current was measured in two separate modes, high and low. ICCH was the supply current measurement with VCC set at 5.5V (maximum supply voltage) and all inputs grounded. The average high level supply current exhibited slightly decreasing magnitude with increasing

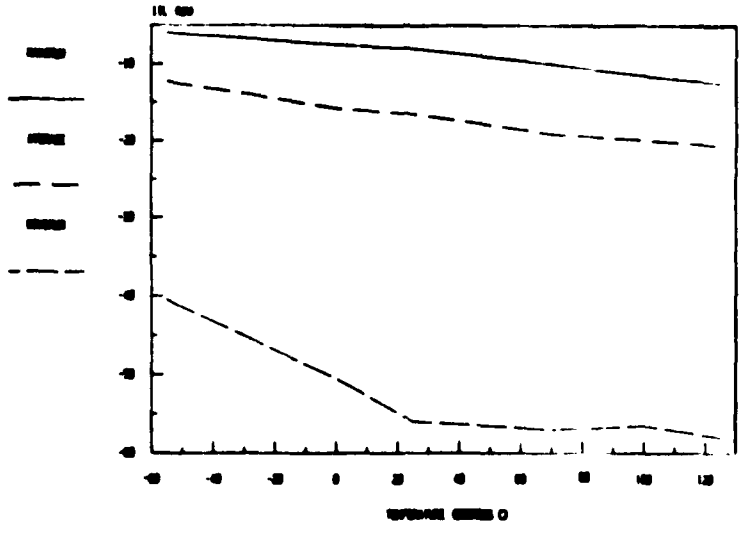


Figure 8.3 Vendor B - Low Level Input Leakage Current

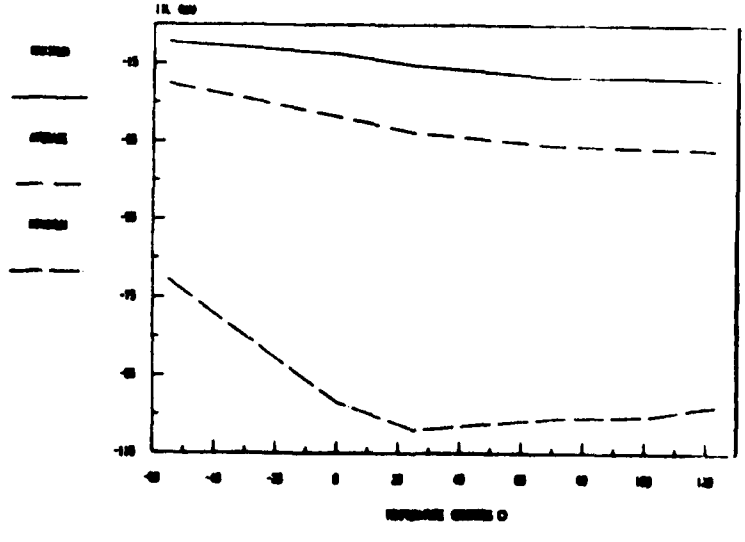


Figure 8.4 Vendor F - Low Level Input Leakage Current

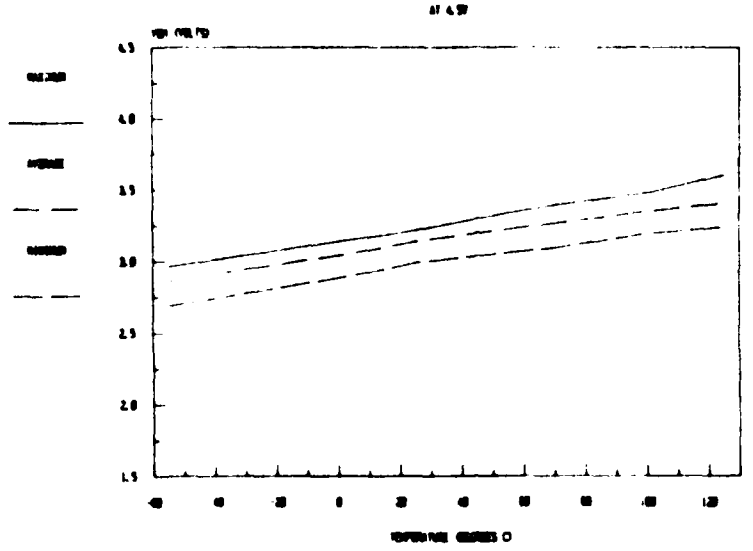


Figure 8.5a Vendor B - High Level Output Voltage (VCC = 4.5V)

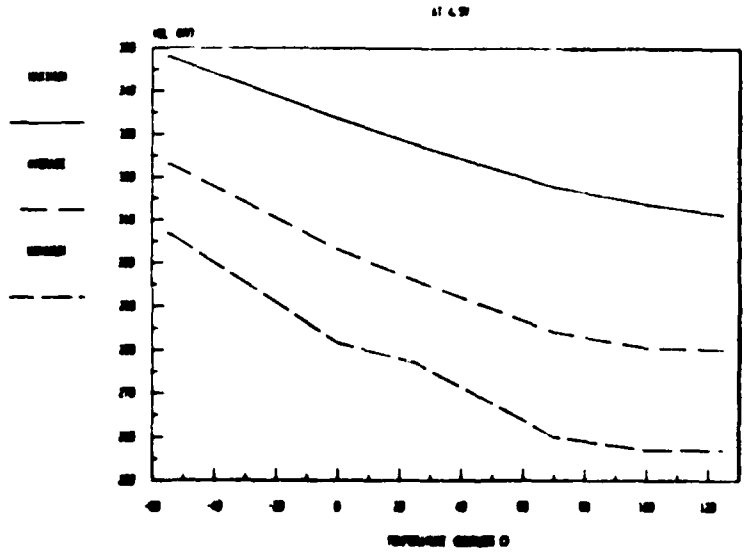


Figure 8.5b Vendor B - Low Level Output Voltage (VCC = 4.5V)

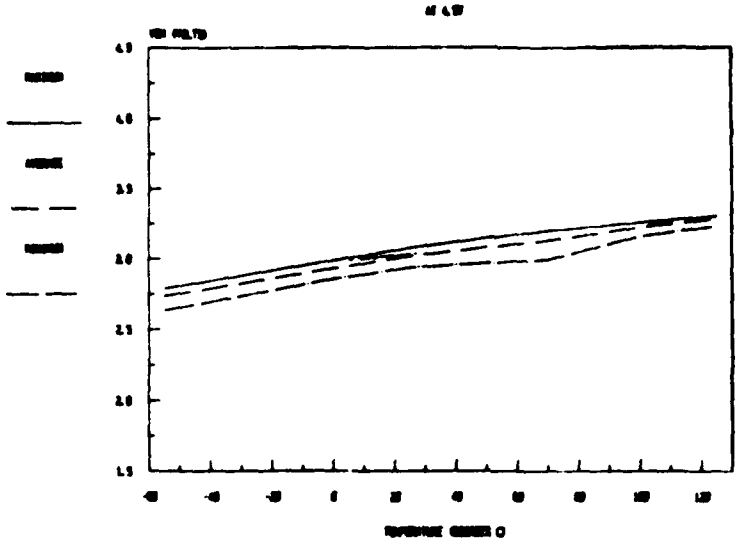


Figure 8.6a Vendor F - High Level Output Voltage (VCC = 4.5V)

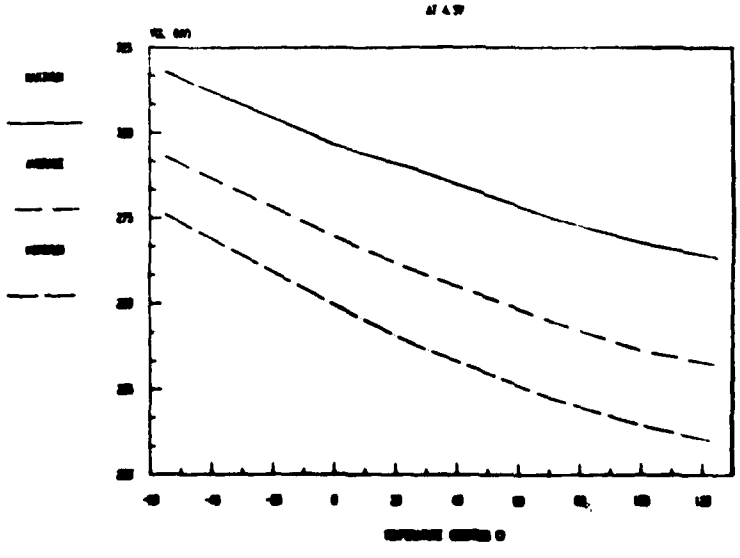


Figure 8.6b Vendor F - Low Level Output Voltage (VCC = 4.5V)

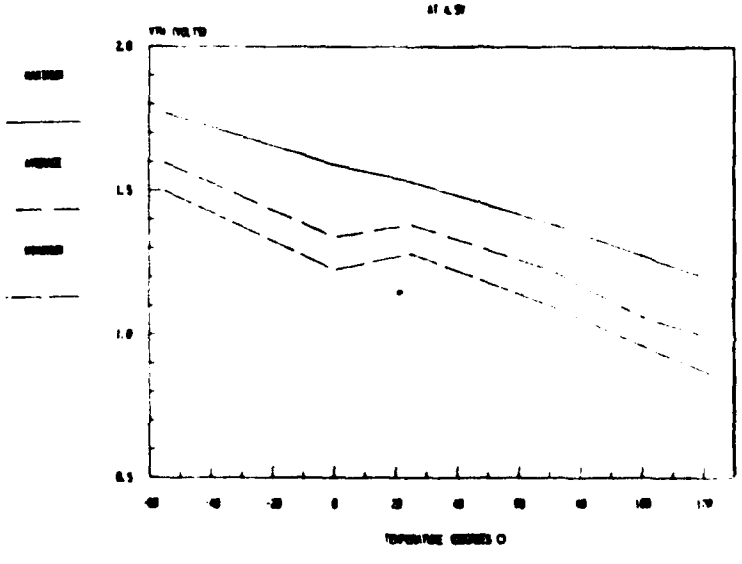


Figure 8.7 Vendor B - Input Voltage Threshold (VCC = 4.5V)

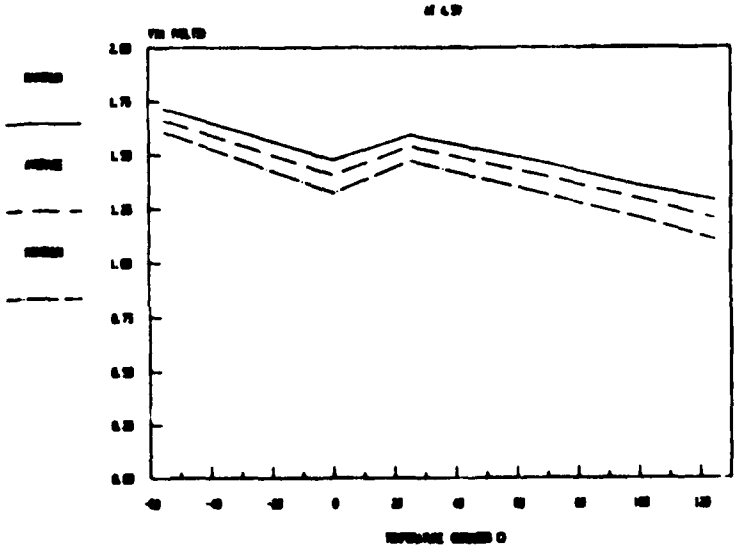


Figure 8.8 Vendor F - Input Voltage Threshold (VCC = 4.5V)

temperature(See Figures 8.9 and 8.10). All data was well below the maximum specified supply current of 180mA with the average current being 145mA. Supply current low level (ICCL) was measured with a VCC of 4.5V and averaged approximately 110mA.

8.3.5 Input Clamp Diode Voltage (VIC)

The input clamp diode voltage measurements were effected by forcing a current of 18mA out of the clamping diode and measuring the voltage across it. The resulting data exhibited a classical curve over temperature which is characterized by extreme linearity and increasing voltage with increasing temperature(Figures 8.11 and 8.13). Again, this is due to the P-N junction's direct proportionality to temperature in degrees kelvin. The average slope of this curve for both vendors was 1.2mV/ C. The vendor specified limit of -1.5V maximum is sufficient with the worst case maximum value being -900mV at -55°C.

8.3.6 Output Short Circuit Current (IOS)

The minimum vendor specification of -30mA appears to be somewhat marginal while the maximum of -130mA is quite liberal with the maximum measured value being -70mA at -55°C and increasing (more positive) with increasing temperature(See Figures 8.12 and 8.14). Overall, the average output short circuit current values were well within the specified vendor limits over the full mil temp range.

8.3.7 I/O Capacitance

I/O capacitance measurements were taken on each input and input/output pin of all devices at a frequency of 1 MHz. Each measurement was made with respect to the ground pin on the device with no supply voltage applied. Table 8.4a and 8.4b are representations of I/O capacitance measurements for selected Vendor F and Vendor B devices:

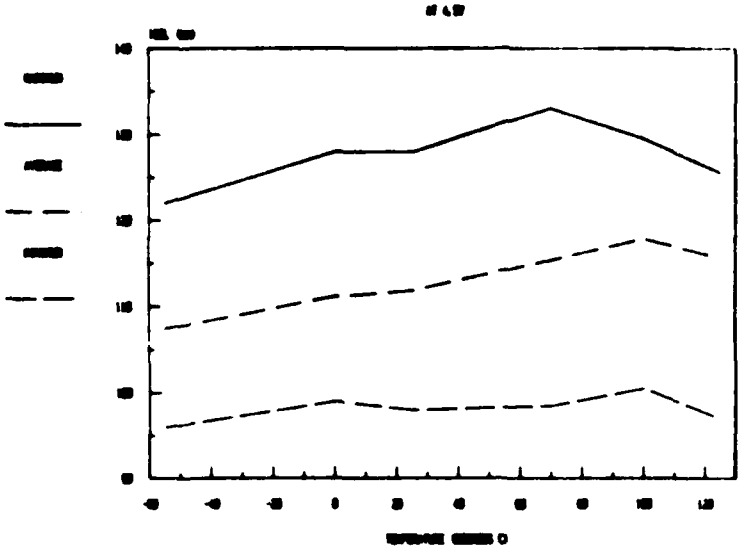


Figure 8.9a Vendor B - Low Level Supply Current (VCC = 4.5V)

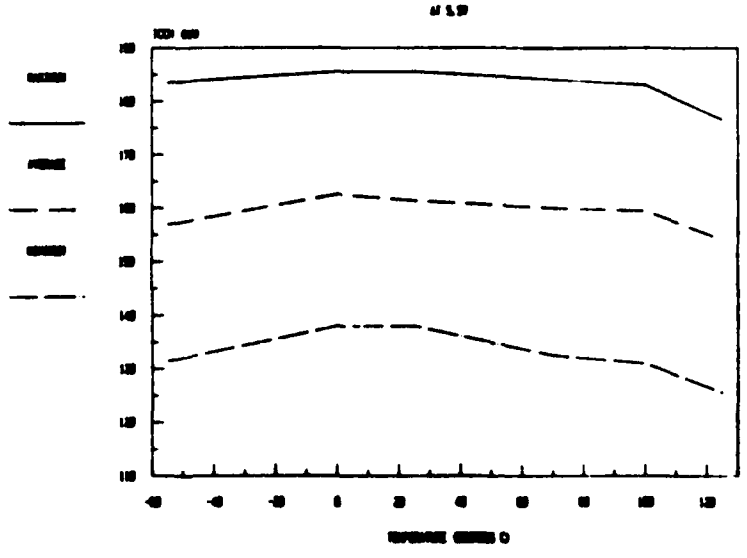


Figure 8.9b Vendor B - High Level Supply Current (VCC = 5.5V)

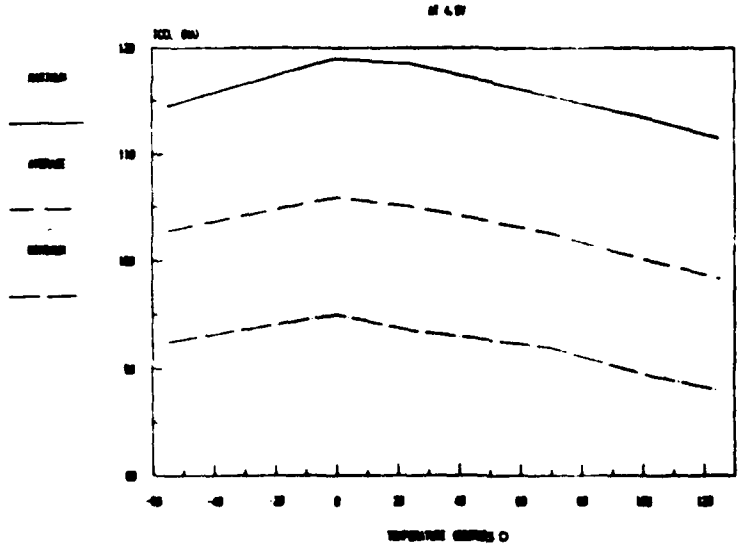


Figure 8.10a Vendor F - Low Level Supply Current (VCC = 4.5V)

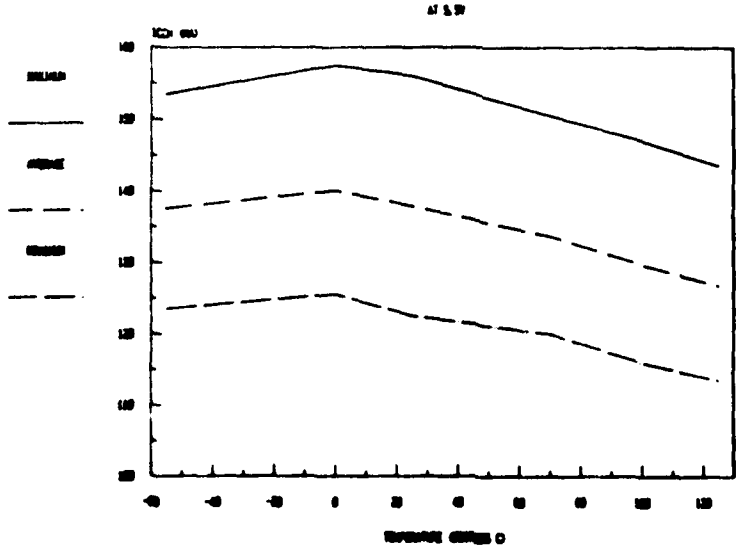


Figure 8.10b Vendor F - High Level Supply Current (VCC = 5.5V)

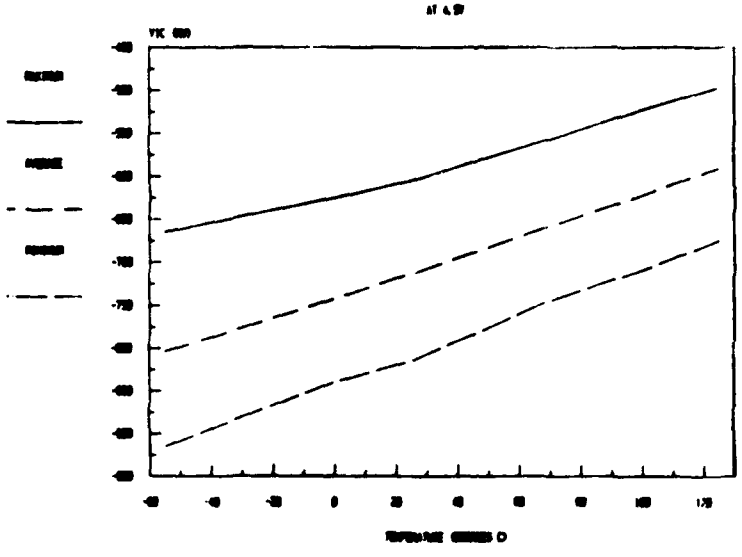


Figure 8.11 Vendor B - Input Clamp Diode Voltage (VCC = 4.5V)

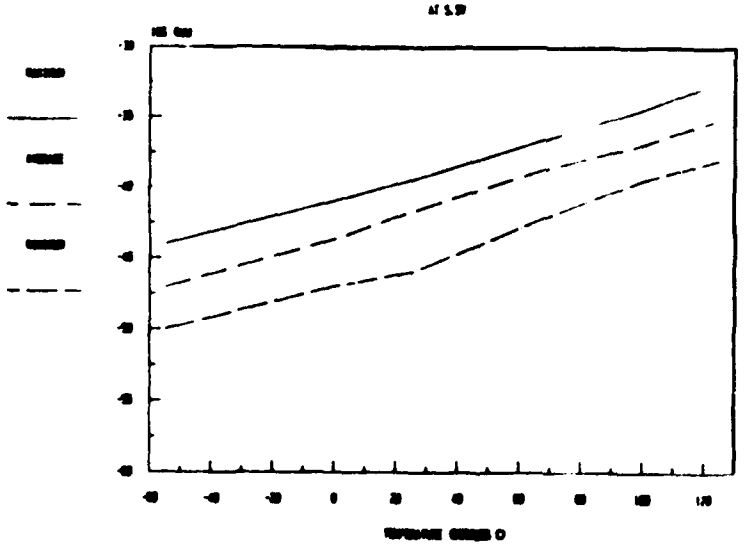


Figure 8.12 Vendor B - Output Short Circuit Current (VCC = 5.5V)

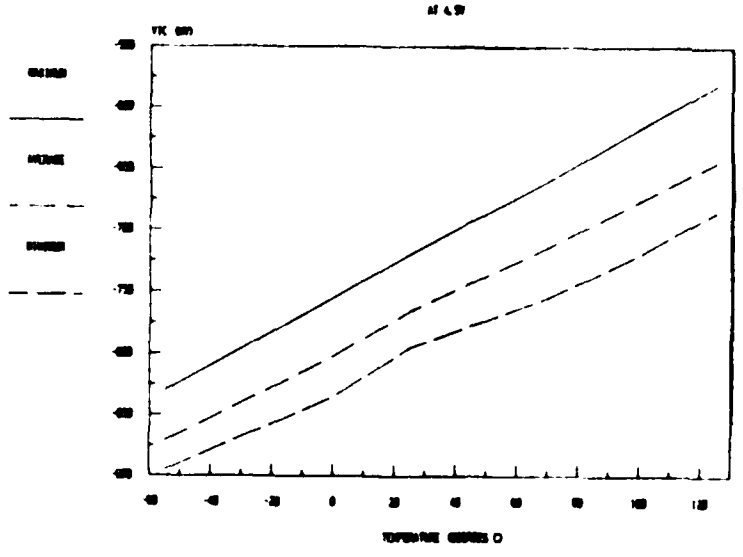


Figure 8.13 Vendor F - Input Clamp Diode Voltage (VCC = 4.5V)

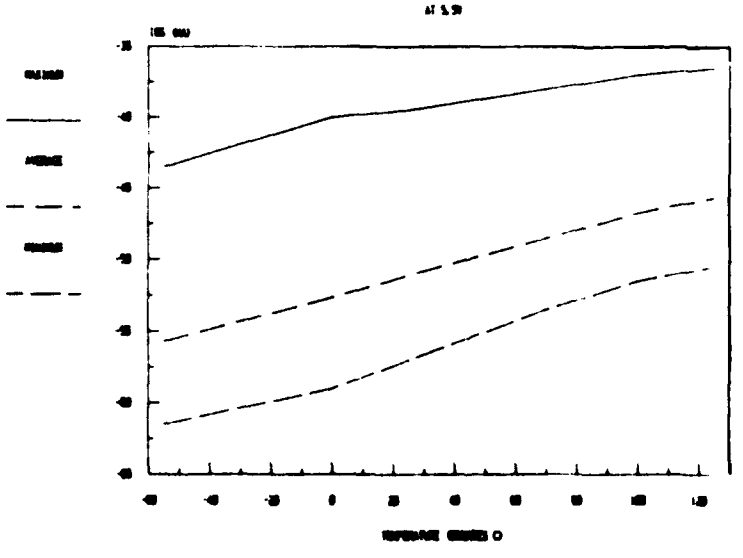


Figure 8.14 Vendor F - Output Short Circuit Current (VCC = 5.5V)

Table 8.4a - Vendor B - I/O Capacitance

Pin #	S/N = 21	S/N = 26	S/N = 36	Max Limit	Unit
1	22.5	23	22.5	Not Available	pf
2	13	13	13		
3	10.7	10.8	10.5		
4	9.1	9	8.9		
5	7.9	7.9	7.8		
6	7.8	7.9	7.7		
7	9	9	8.8		
8	10.6	10.8	10.5		
9	14	14	13.6		
11	22.4	24	23.3		
12	20	20.5	20		
13	12.1	12.6	12.5		
14	10.5	10.6	10.6		
15	10	10.3	10.1		
16	10	10.3	10.2		
17	10.5	10.7	10.7		
18	12.5	12.6	12.7		
19	20.8	20.7	20.4		

Table 8.4b - Vendor F - I/O Capacitance

Pin #	S/N = 50	S/N = 60	S/N = 64	Max Limit	Unit
1	18.5	17.5	18	Not Available	pf
2	10.5	10.1	10.5		
3	8.7	8.4	8.6		
4	8.3	8.1	8.5		
5	7.7	7.5	7.7		
6	7.8	7.4	7.8		
7	8.2	7.9	8.3		
8	8.6	8.2	8.5		
9	12	11.5	12		
11	18	18.4	18		
12	24	24	22.6		
13	11	11	11.5		
14	10.5	10	10.5		
15	10.3	10	10.5		
16	10.4	10.2	10.4		
17	10.4	10.3	10.5		
18	11.3	11.1	11.2		
19	16.5	16.1	16.3		

8.4 AC Parameters

The AC characterization of the PAL16R8 was accomplished utilizing the following parameters and conditions as shown in Table 8.5.

Table 8.5 AC Parameters for the PAL16R8 (Vendors B and F)

Parameter	Symbol	Min	Max	Units
Clock Pulse Width High	TCHCL	25	---	nsec
Clock Pulse Width Low	TCLCH	25	---	
Input to Clock Setup Time	TCHAV	45	---	
Input to Clock Hold Time	TCHAX	0	---	
Clock High to Data Valid	TCHDV	---	25	
Output Buffer Turn-on Time	TOLQX	---	25	
Output Buffer Turn-off Time	TOHQZ	---	25	
Maximum Operating Frequency	fmax	14	---	MHZ

8.4.1 Maximum Operating Frequency

Minimum period measurements were derived as the sum of TCHCL and TCLCH(See Figures 8.15 and 8.16). At 25°C the maximum operating frequency of the PAL16R8 increases with increasing VCC. The average maximum frequency ranges from approximately 32MHz at VCC = 4.25V to 40MHz at VCC = 5.75V with a nominal maximum frequency of approximately 37MHz at 5.0 Volts VCC. This is significantly better than the minimum specified frequency of 14MHz as indicated in slash 504. The trend at -55 C is similar although slightly less pronounced with the average maximum frequency ranging from 2MHz at 4.25V VCC to approximately 36MHz at VCC = 5.75V. The data at 125°C exhibits a significantly flatter curve with the average maximum at 4.25V VCC being 26MHz and 24MHz at VCC = 5.75V.

8.4.2 Address Setup Time

TCHAV (Setup time) for the PAL16R8 is defined as the time a stable address is required at the inputs before the output registers may be clocked. The general trend is for decreasing setup time with increasing

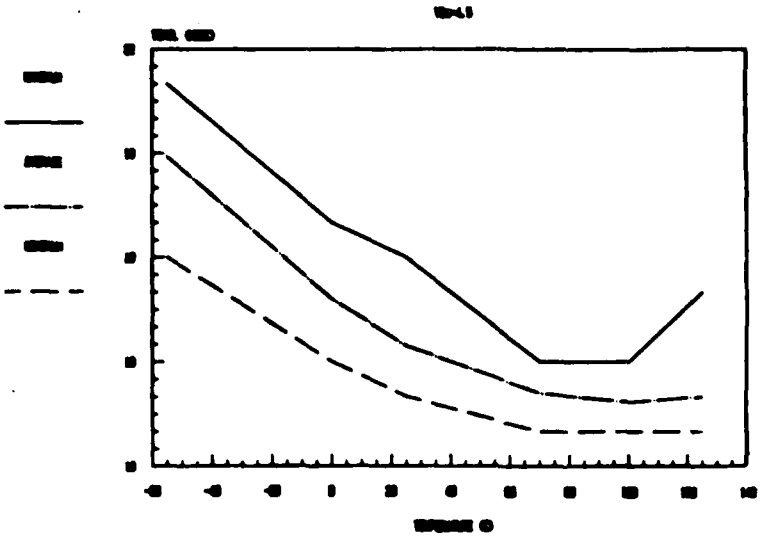


Figure 8.15a Vendor F - Clock Pulse Width High (VCC = 4.5V)

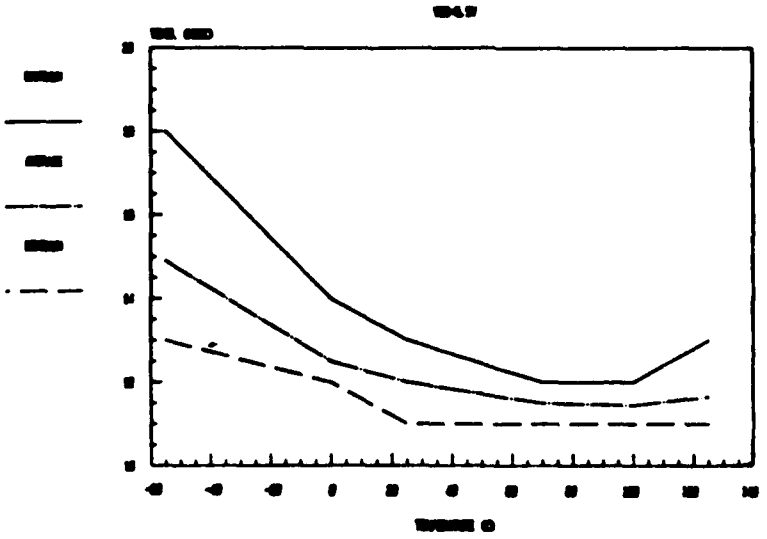


Figure 8.15b Vendor F - Clock Pulse Width High (VCC = 5.5V)

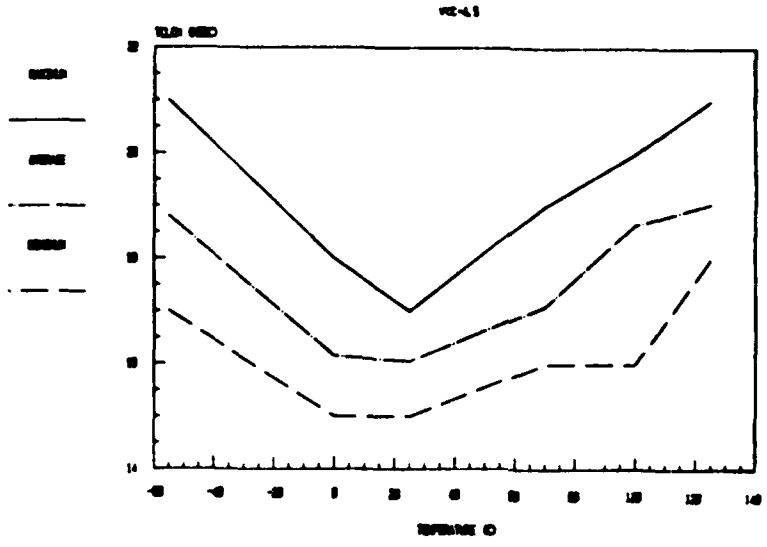


Figure 8.16a Vendor F - Clock Pulse Width Low (VCC = 4.5V)

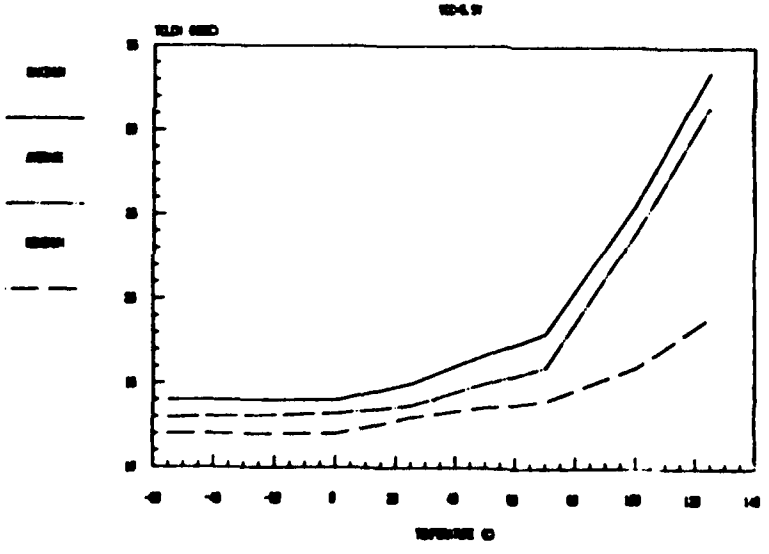


Figure 8.16b Vendor F - Clock Pulse Width Low (VCC = 5.5V)

VCC. This is as expected since the major contributor to setup time is the propagation delay through the device. At 25°C the average setup time ranges from 26 nsec at VCC = 4.25 Volts to 20 nsec at VCC = 5.75V in a relatively linear fashion(See Figure 8.17). At -55°C the values are slightly higher with TCHAV being 30 nsec at VCC = 4.25V to 21 nsec at VCC = 5.75 Volts; again, a relatively linear curve. The curve at 125°C is somewhat compressed with setup times of 28 nsec to 25 nsec for supply voltages of 4.25 Volts to 5.75 Volts respectively. Over the military temperature range all values were well within the maximum allowable setup time of 45 nsec.

8.4.3 Address Hold Time

TCHAX (Address Hold Time) is the time that a stable address is required to exist after the application of the output register clocking pulse. Typically, hold times are negative due to the finite decay time of internal circuit nodes. Again, the hold time vs. supply voltage curves over the military temperature range are relatively linear(See Figure 18). The slopes are positive indicating an increasing hold time for increasing VCC. At 25°C hold times vary from -22nS at 4.15V VCC to -17nS at 5.75V VCC. At 55°C the slope was slightly steeper with an 8nS variation over the VCC range, i.e., -23nS to -15nS for VCCs of 4.25V to 5.75V. The data for 125°C is over the supply voltage range. All values easily meet the 0 nsec minimum requirement for address hold time and are significantly better than the -15 nsec typical value specified in the vendor data sheets.

8.4.4 Clock High to Data Valid

TCHDV (Clock High to Data Valid) is essentially an access time measured from the leading clock edge to valid data out. All TCHDV measurements were below the vendor specified maximum limit of 25 nsec over the full military temperature range. Over the VCC range (4.25 Volts to 5.75 Volts) TCHDV varied from 16 nsec to 20 nsec at 25°C (See Figure 8.19). At -55°C the slope of the curve was less steep with an excursion from 23 nsec to 21 nsec for increasing VCC. TCHDV was a flat curve with less than a 1 nsec variation at 125°C.

8.4.5 Output Buffer Turn-on Time

TOLQX is output buffer turn-on time and is defined as the time from the output disable (OD-Pin #11) rising edge to a valid data output. The data at 25°C exhibits a negatively sloped curve with decreasing turn-on time for increasing VCC(See Figure 8.20). Average values were 16 nsec at 4.25 Volts to 12 nsec at 5.75 VCC. This trend was relatively unaffected by temperature and all values were well within the 25 nsec maximum limit specified by the vendor.

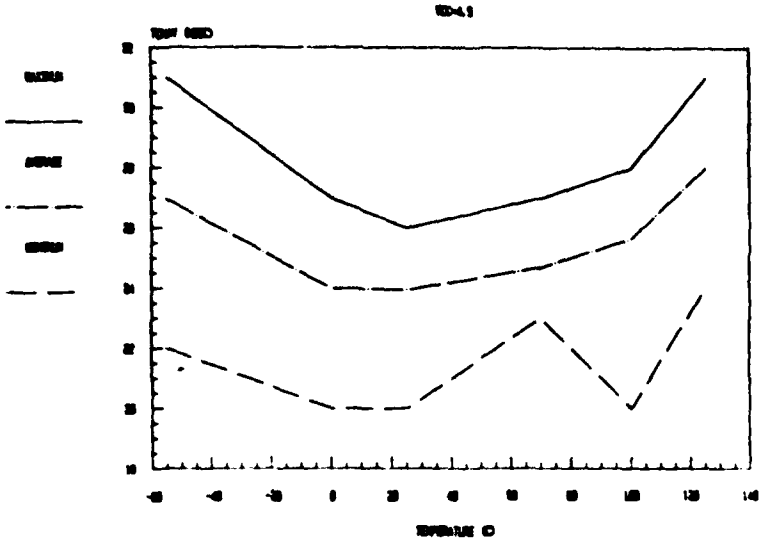


Figure 8.17a Vendor F - Address Setup Time (VCC = 4.5V)

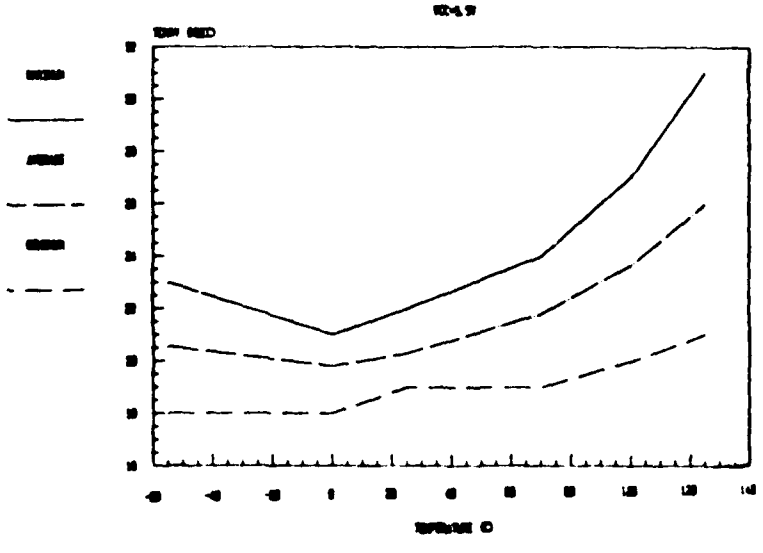


Figure 8.17b Vendor F - Address Setup Time (VCC = 5.5V)

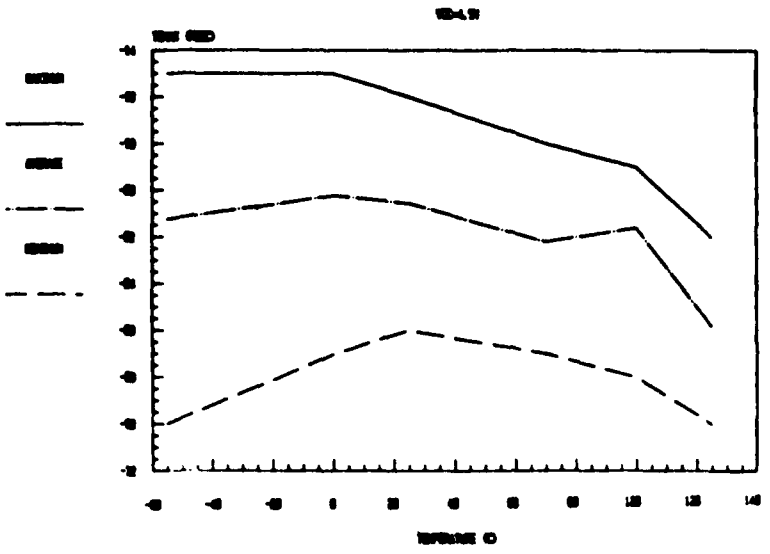


Figure 8.18a Vendor F - Address Hold Time (VCC = 4.5V)

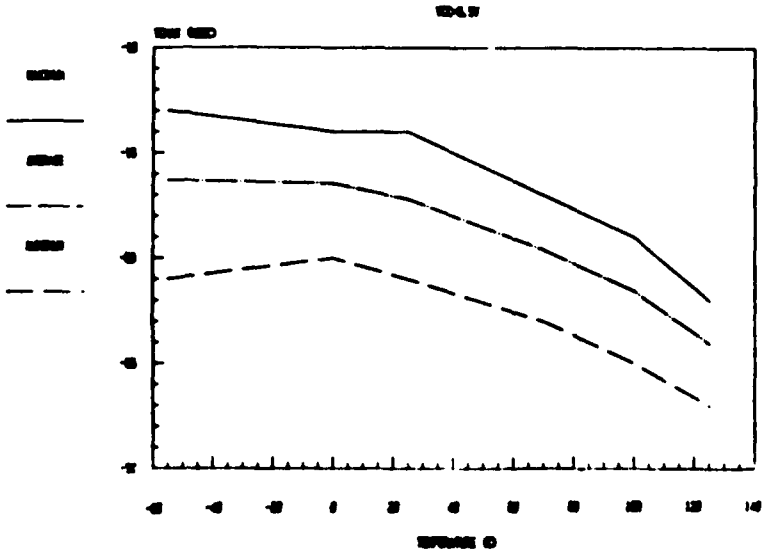


Figure 8.18b Vendor F - Address Hold Time (VCC = 5.5V)

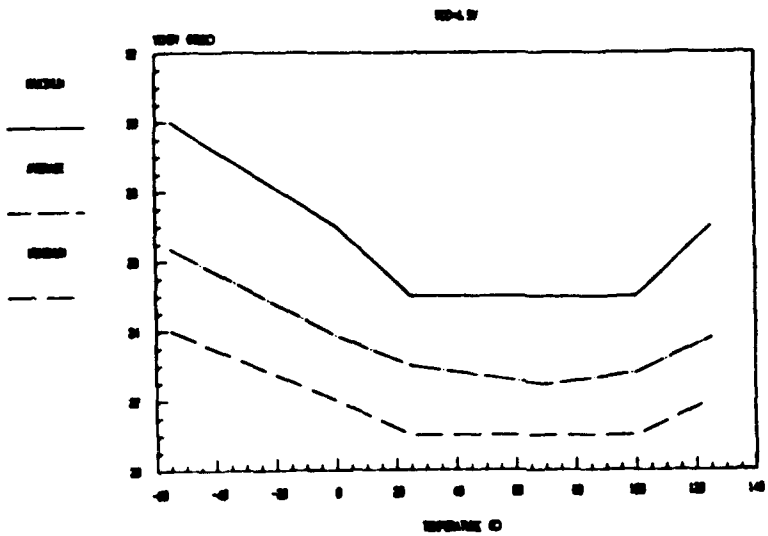


Figure 8.19a Vendor F - Clock High to Data Valid Access Time (VCC = 4.5V)

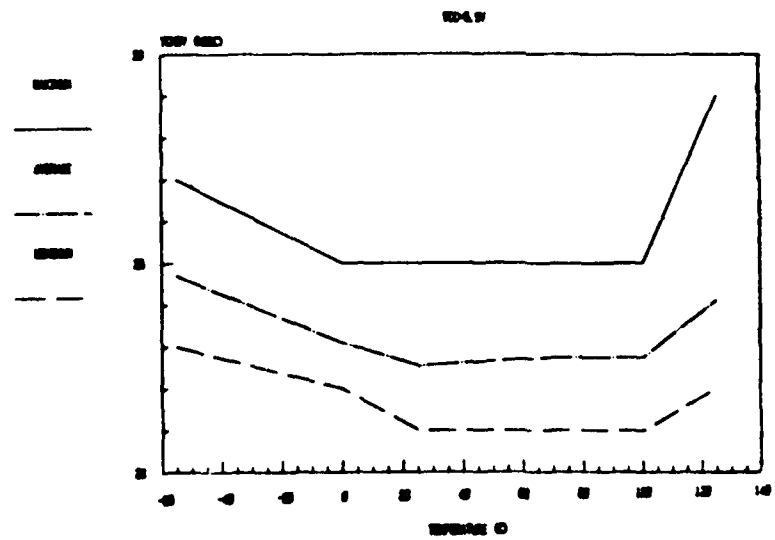


Figure 8.19b Vendor F - Clock High to Data Valid Access Time (VCC = 5.5V)

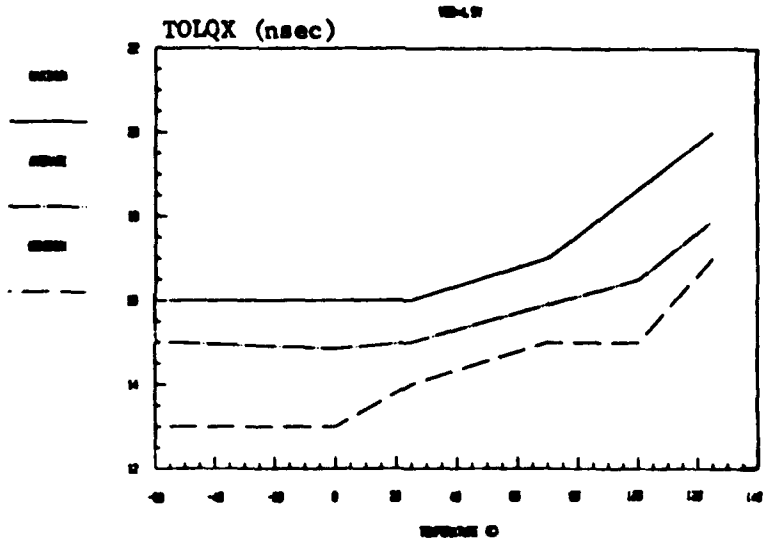


Figure 8.20a Vendor F - Output Buffer Turn-on Time (VCC = 4.5V)

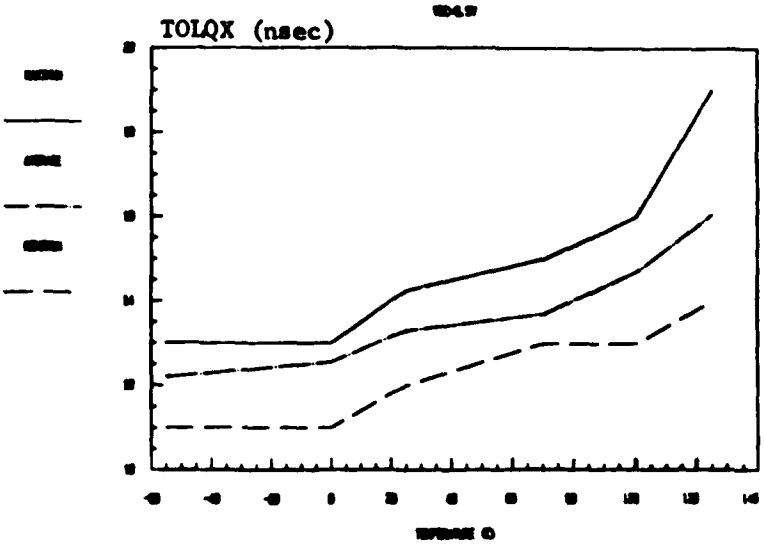


Figure 8.20b Vendor F - Output Buffer Turn-on Time (VCC = 5.5V)

8.5 Programming Parameters

Prior to the characterization of the PALS, they were programmed on the S-3270 by applying nominal programming parameters. To characterize the devices, they were programmed with the minimum programming parameters given in Table 8.6. These parameters were reduced by 10% each pass until a device failed to program.

Table 8.6 Programming Parameters for the PAL16R8 (Vendors B and F)

Parameters	Symbol	Min	Max	Units
Program Level Input Voltage	VIHH	---	12	Volts
Program Level Input Current	IIHH			
Output program pulse		---	50	mA
O/D, L/R		---	25	mA
All other inputs		---	5	mA
Program Supply Current	ICCH	---	400	mA
Program Pulse Width	TPHPL	10	50	usec
	td	100	---	nsec

The two timing parameters that were varied were td, delay time, and tp, the width of the programming pulse. The voltage parameter that was varied was VIHH, the program level input voltage. These parameters were varied independently with the fixed parameter set at the specified minimum value, i.e. while characterizing the timing parameters, VIHH was set at 11.0 volts and while varying VIHH, td and tp were set to 100 nsec and 10 usec respectively. The results of this characterization is as follows: Vendor B, S/N 72, programmed at the minimum specified timing setting of td = 100 nsec and tp = 10 usec. Vendor B, S/N's 76 and 77, programmed at 10% below minimum. S/N's 73 and 75 failed to program at 20% below minimum. Vendor B, S/N's 74 and 78 failed to program with VIHH set 10% below the minimum specified limit of 11.0 volts. For Vendor F, S/N 1P programmed at the minimum specified programming parameters. S/N's 2P and 3P programmed at 20% below and 50% below the minimum specified timing respectively. S/N's 4P and 5P both failed to program with VIHH set to 10% below minimum (i.e. 9.9 volts). This data indicates that programming is sensitive to the program-level input voltage but relatively insensitive to program timing constraints. Since all devices programmed at minimum timing and voltage level parameters, the vendor programming specifications are adequate.

APPENDIX A - Test Plan Example

1.0 Procurement

A minimum of 20 devices of each type will be procured and tested. Since 15 devices are required by the contract, the extra devices will allow some fall-out to occur without having to repeat testing for replacements. The vendors selected will be per discussion between RADC and GE. To aid in subsequent test development, a bit map for each device type will be requested from the manufacturer.

2.0 Incoming Test

The devices will be tested on the Tektronix to verify continuity of the programmable links and logic integrity of the unprogrammed outputs.

The incoming test will not verify all DC parameters, but will detect gross failures. The DC characterization which follows this initial testing will serve to complete the function of incoming testing as well as to profile the DC performance of each device.

3.0 DC Characterization

Data patterns used here will be those developed for AC functional testing.

The following DC parameters will be measured at various temperatures that will include as a minimum -55, 25, and 125°C. Other conditions as indicated will also be applied.

3.1 Supply Current

The VCC supply will be measured with VCC = 5.5V.

3.2 Input Current

The input current of all input pins will be measured at VIN = 0.0, 0.4, 2.4, and VCC. The VCC supply voltage will be set to 5.5V.

3.3 Input Clamp Voltage

The forward bias voltage of the input protection diodes will be measured while forcing the maximum specified bias current.

3.4 Output Leakage

For those devices with tri-state outputs, the output current will be measured while all outputs are disabled and VCC = max. The measurement will be performed while externally applying 0.0, 0.4, 2.4, and VCC to the output.

3.5 Output Voltage

VOH - Output logic high voltage will be measured while the output is sourcing the manufacturer's maximum specified current.

VOL - Output logic low voltage will be measured while the output is sinking the manufacturer's maximum specified current.

3.6 Input/Output Capacitance

The capacitance of all input/output pins on a minimum of five devices will be measured at a frequency of 1MHz.

3.7 Output Short Circuit Current

With the output initially in the logic high state and VCC at maximum, the output will be momentarily shorted to ground while measuring the current sourced by the output. This test will be followed by a second set of output voltage tests to insure that no damage resulted from the short circuit condition.

3.8 Input Thresholds

The switching thresholds of at least three device inputs will be determined at -55, 25, and 125°C with VCC = 4.5, 5.0, and 5.5V.

The measurement technique will use VIH and VIL levels of 3.0 and 0.0 volts respectively on all those pins not currently selected for threshold measurement. When determining the VIH threshold for the selected pin, VIL will be at 0.0 volts. An input pattern will be applied to the inputs while monitoring outputs for correct logic states and response times. For each execution of the pattern VIH, on the selected pin, will be incrementally increased until the value is found at which the device passes.

When VIL threshold is being determined, VIH on the selected pin will be set to 2.0 volts. VIL then will be incrementally decreased at each execution of the pattern until the device passes.

The threshold tests will be performed at -55, 25, and 125°C with VCC = 4.5, 5.0, and 5.5 volts.

4.0 AC Characterization

The AC parameters will be measured under various temperature and voltage conditions that will include the following as a minimum unless otherwise indicated:

Temperature = -55, 25, and 125°C

VCC = 4.25, 4.50, 4.75, 5.0, 5.25, 5.5, and 5.75V
VIH = 2.0, 2.4, 3.0V
VIL = 0.8, 0.6, 0.4V

The output voltage compare levels will be set at the manufacturer specified minimum VOH and VOL limits.

The parameters that will be measured are:

a.) maximum propagation time of the input to output asynchronous data paths
b.) maximum propagation time of clock inputs
c.) clock widths
d.) setup times
e.) hold times
f.) maximum clock frequency of synchronous circuits - In the event the maximum clock frequency exceeds the automatic test equipment capability, a bench test will be performed at limited VCC and logic levels.

The AC parameters will be measured using selected patterns. Since each device can have only one of the selected patterns not all propagation delays can be verified in a single device. However, the various patterns used will collectively verify the propagation integrity of the device design and will verify that any fuse can be programmed.

A load circuit, as shown in Figure 2.3 in section 2 will be connected to each output during the AC testing. Resistor RL will be selected to provide the maximum load current at the maximum allowed output logic low voltage. RH will provide maximum load current for the minimum allowed logic high output voltage. The 50pF capacitance includes the parasitic capacitance of the test equipment.

5.0 Programming Characteristics

The proposed plan for the programmable logic devices is to select various programming parameter values within the manufacturer's specified minimum and maximum values and sufficiently below the minimum values to verify that the limits are adequate. The maximum values will not be exceeded to avoid damage to the devices.

The characterization will apply various combinations of the following parameters to each device (within the limits of the programming hardware):

program level input voltage
program pulse width
delay time from programming voltage to programming pulse
verify protect input voltage
verify protect pulse width

In addition, the program supply current, program level input current and verify protect input current will be measured while programming selected fuses in at least five different devices.

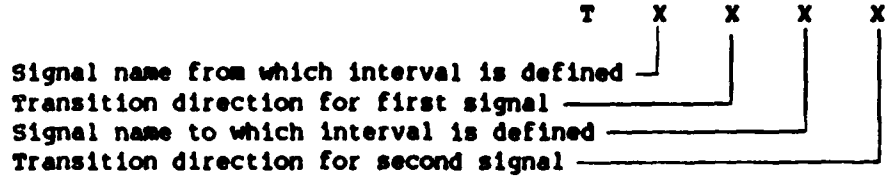
6.0 Burn-In

The effect of the programming parameters is assigned to some extent by pattern verification. However, a burn-in period is recommended to provide a more rigorous set of conditions for checking the integrity of the open fuse. This is especially important here, because many fuses will receive minimum program parameters possibly resulting in an incomplete fuse burn. A minimum of 160 hours of dynamic burn-in is suggested. An additional burn-in (life test) can be performed if time and schedule permits.

APPENDIX B - Special Diagrams and Definitions

Timing parameter abbreviations-

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transition. Thus the format is:



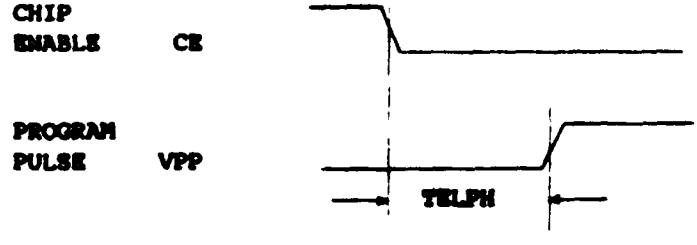
a. Signal definitions:

A=Address
D=Data in
Q=Data out
E=Chip-enable
O=Output-enable
P=Program (VPP) pulse

b. Transition definitions:

H=Transition to high
L=Transition to low
V=Transition to valid
X=Transition to invalid or don't care
Z=Transition to off (high impedance)

Example:



The example shows Chip-enable setup time defined as TELPH time from chip-enable low to program pulse high.

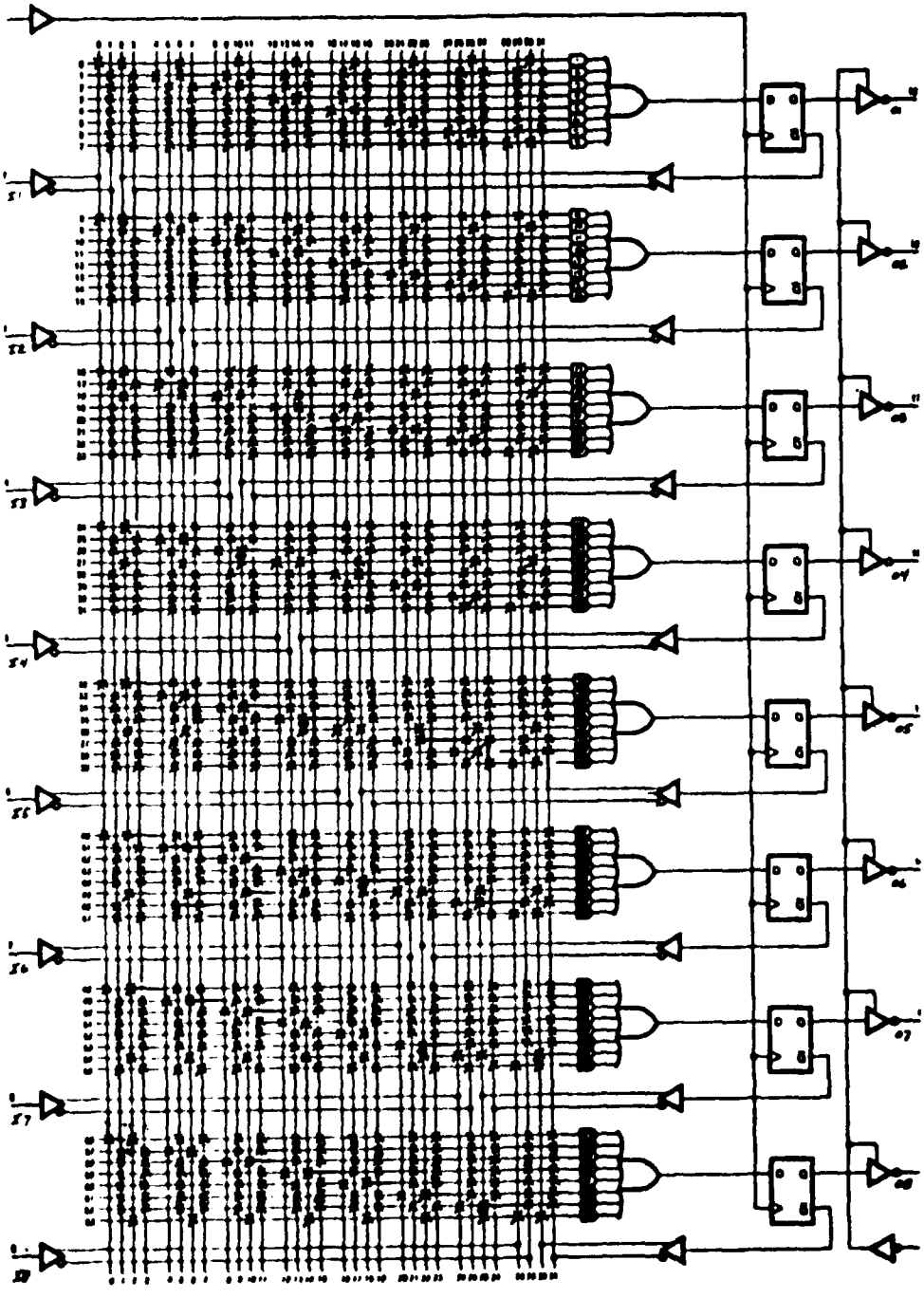


Figure B.1 PAL16R8 - Fuse Pattern #1

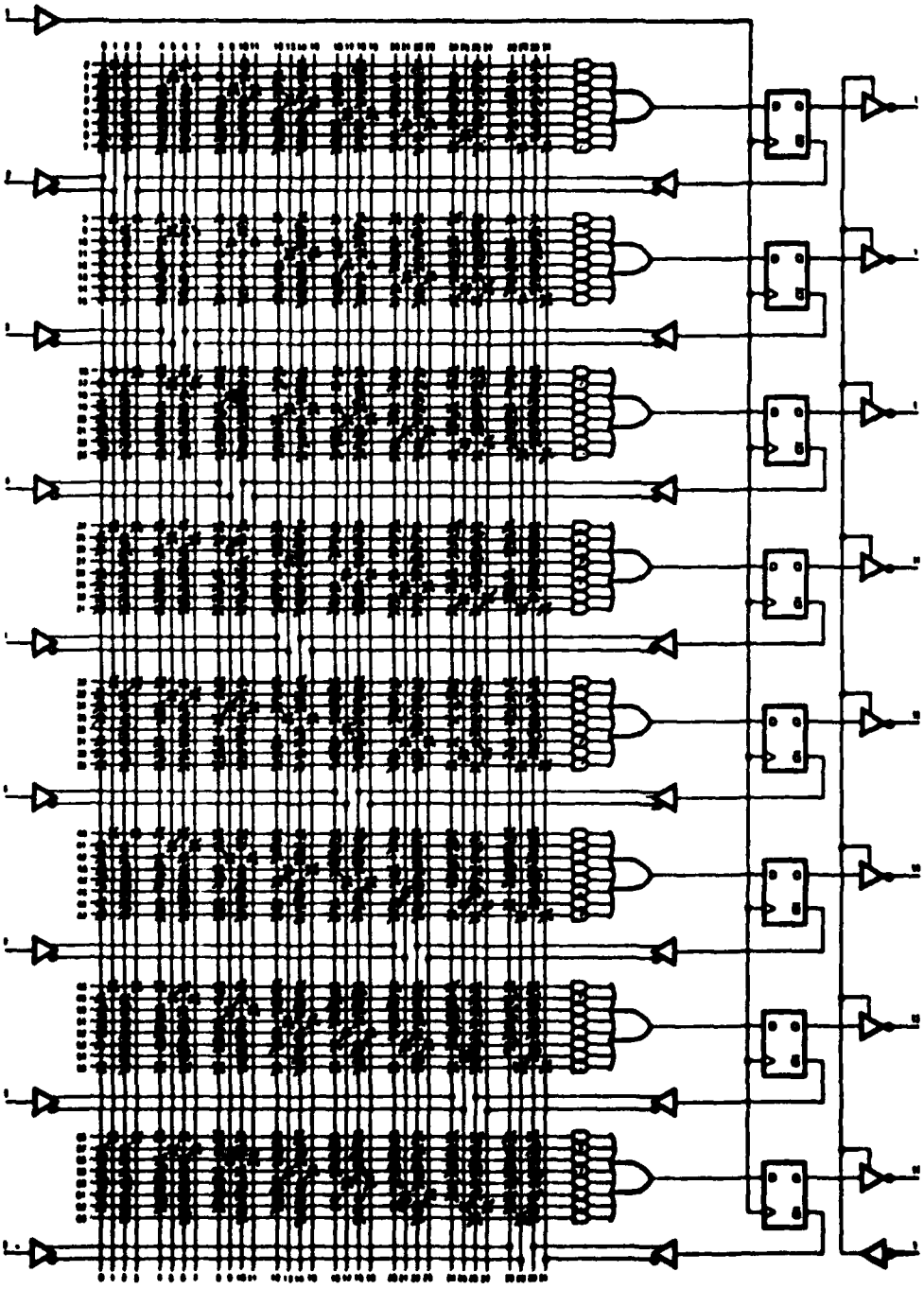


Figure B.2 PAL16R8 - Fuse Pattern #2

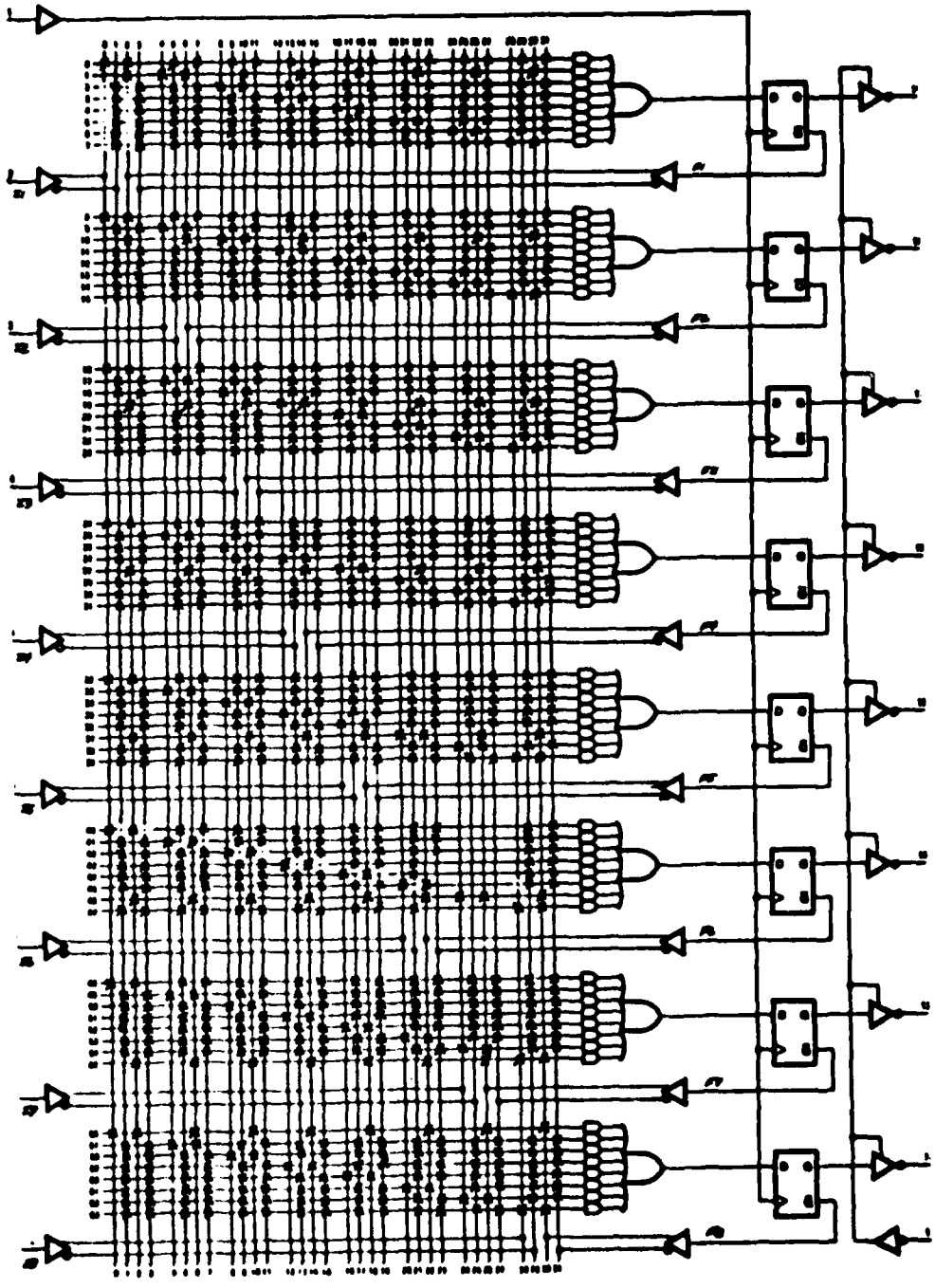


Figure B.3 PAL16R8 - Fuse Pattern #3

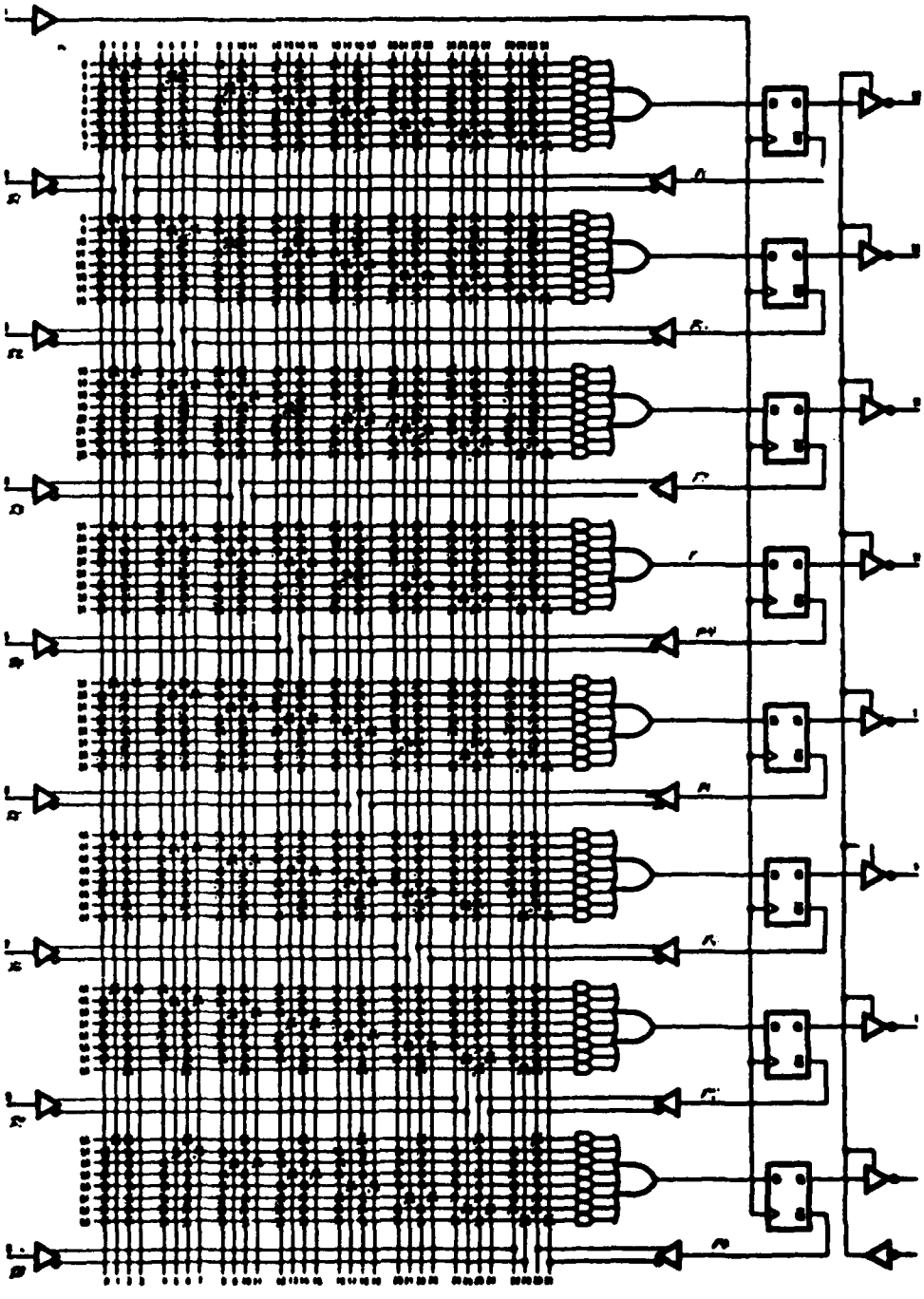


Figure B.4 PAL16R8 - Fuse Pattern #4

APPENDIX C - Data Pattern Descriptions

Marching Pattern - RAM

This pattern is used to test for bit independence and address uniqueness. A variation of the pattern is also used to check that data cannot be written into the device when it is deselected. The basic March pattern is performed in the following sequence:

Step 1 - Write the array with background data.
Step 2 - Read the entire memory for background data.
Step 3 - Read address location zero for background data.
Step 4 - Write address location zero with complement data.
Step 5 - Read address location zero for complement data.
Step 6 - Repeat steps 3 through 5 for each address location.
Step 7 - Repeat steps 3 through 6 using complement data and addresses the decrement from maximum.
Step 8 - Repeat steps 3 through 7 with complement data.

When verifying that data cannot be written while the chip is deselected, the pattern is performed in the following sequence:

Step 1 - Write the array with background data.
Step 2 - Read the entire memory for background data.
Step 3 - Read address location zero for background data.
Step 4 - Deselect the device and attempt to write complement data at location zero.
Step 5 - Read address location to verify that complement data was not written into location zero.
Step 6 - Repeat steps 3 through 5 for all addresses.
Step 7 - Repeat steps 1 through 7 with complement data.

Marching Pattern - ROM

Step 1 - Starting with address zero, read all addresses in increasing sequential order.
Step 2 - Starting with the maximum address, read all addresses in decreasing sequential order.

Address Complement Pattern - RAM

Step 1 - Write 1s and 0s alternately into the array.
Step 2 - Read 1s at address location zero.
Step 3 - Write 0s at address location zero.
Step 4 - Read 0s at complement address location.
Step 5 - Write 1s at this address location.
Step 6 - Read 0s at address location one.
Step 7 - Write 1s at address location one.
Step 8 - Read 1s at the complement address location.
Step 9 - Write 0s at this address location.
Step 10 - Repeat steps 2 through 9 until finished with every address in the array.
Step 11 - Read out data pattern from memory.
Step 12 - Repeat steps 1 through 11 with complement data.

Address Complement Pattern - ROM

Step 1 - Read data at address zero.
Step 2 - Read data at complement address.
Step 3 - Read data at address one.
Step 4 - Read data at complement address.
Step 5 - Continue sequence until all addresses have been read.

Row Complement Pattern - RAM

Step 1 - Write 1s and 0s alternately within each column.
Step 2 - Read 1s at the first row address in the first column.
Step 3 - Write 0s at the same location.
Step 4 - Read 0s at the complement row address location in the same column.
Step 5 - Write 1s at this complement row address location.
Step 6 - Read 0s at the second row address location.
Step 7 - Write 1s at the second row address location.
Step 8 - Read 1s at the complement-second-row address location.
Step 9 - Write 0s at this complement-second-row address location.
Step 10 - Repeat steps 2 through 9 until finished with every row address in that column.
Step 11 - Repeat steps 2 through 10 for the remaining columns.
Step 12 - Read out data pattern from memory.
Step 13 - Repeat steps 1 through 12 with complement data.

Row Complement Pattern - ROM

Step 1 - Read first row in the first column.
Step 2 - Read the complement row in the first column.
Step 3 - Read the second row in the first column.
Step 4 - Read the complement row in the first column.
Step 5 - Continue the sequence until all rows in the first column have been read.
Step 6 - Repeat steps 1 through 5 at each column in each row until the entire memory has been read.

Column Complement Pattern - RAM

Step 1 - Write 1s and 0s alternately within each row.
Step 2 - Read 1s at the first column address in the first row.
Step 3 - Write 0s at the same location.
Step 4 - Read 0s at the complement column address location in the same row.
Step 5 - Write 1s at this complement column address location.
Step 6 - Read 0s at the second column address location.
Step 7 - Write 1s at the second column address location.
Step 8 - Read 1s at the complement-second-column address location.
Step 9 - Write 0s at this complement-second-column address location.
Step 10 - Repeat steps 2 through 9 until finished with every column-address in that row.
Step 11 - Repeat steps 2 through 10 for the remaining rows.
Step 12 - Read out data pattern from memory.
Step 13 - Repeat steps 1 through 12 with complement data.

Column Complement Pattern - ROM

Step 1 - Read first column in the first row.
Step 2 - Read complement column in the first row.
Step 3 - Read second column in the first row.
Step 4 - Read complement column in the first row.
Step 5 - Continue the sequence until all columns in the first row have been read.
Step 6 - Repeat steps 1 through 5 at each row until the entire memory has been read.

Galloping Address Pattern - RAM

This pattern is used to check memory access time between one address and every other address. It is performed in the following manner:

Step 1 - Write a background pattern throughout the memory.
Step 2 - Read the array for the background pattern.
Step 3 - Select address zero as the test word location.
Step 4 - Write the complement of the background data at the test word location.
Step 5 - Execute the following sequence:

Read the test location
Read the test location +1
Read the test location
Read the test location +2
Read the test location
.
.
.
Continue the sequence until all locations have been read.

Step 6 - Write the background data into the test word location.
Step 7 - Select test word location +1 as the next test word location.
Step 8 - Repeat steps 4, 5, and 6.
Step 9 - Repeat steps 7 and 8 until all addresses have been the test word location.
Step 10 - Repeat steps 1 through 9 with complement background data.

Galloping Address Pattern - ROM

Step 1 - Select address zero as the test location.
Step 2 - Execute the following sequence:

Read the test location
Read the test location +1
Read the test location
Read the test location +2
Read the test location
.
.
.
Continue the sequence until all locations have been read.

Step 3 - Select test location +1 as the next test location.
Step 4 - Repeat step 2.
Step 5 - Repeat steps 3 and 4 until all addresses have been the test location.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